Hands on Experience for Faculty in Laboratories
Phase I
JNTUK, Kakinada

Cover page

Report

Details of College

Name of the College	LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY
College Code and District	KD and VIZIANAGARAM
Name of the Principal	Dr.V.V.RAMA REDDY
Contact No's	

Details of the Department

Name of the Department	ELECTRONICS AND COMMUNICATION ENGINEERING
Name of Head of the Department	Dr.M.RAJAN BABU
Contact No's	9492618186

Details of the Faculty Member

Name of the Faculty Member	V.NANCHARIAH
Qualification and Specialization	M.Tech (VLSISD)
Contact No's	9014945788

Details of the Faculty Member

Name of the Faculty Member	N.RAJASEKHAR, M.SUJATHA
Qualification and Specialization	M.Tech (RADAR & MICROWAVE,SIGNAL & SYSTEM PROCESSING)
Contact No's	9985565990, 8142677038

Details of the Laboratory

Year and Semester of Lab	II YEAR-I SEM
Name of the Laboratory	ELECTRONIC DEVICES AND CIRCUITS
No of Experiments as per syllabus	12
No of Experiments conducted	10

Signature of Faculty Member Signature of HOD Signature of Principal

Hands-on Experience for Faculty in Laboratories

Phase I

Preamble

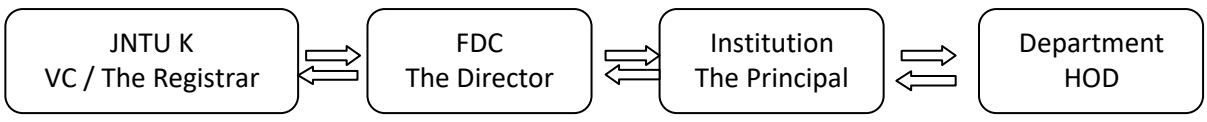
The "**Hands-on Experience for Faculty in Laboratories**" is a faculty development programme conceptualized and designed by the Directorate of Faculty Development, JNTU K under the scholarly guidance of The Hon'ble Vice-Chancellor Prof G Tulasi Ram Das, to address the quality concerns in technical education through empowerment and capacity building of the faculty. The programme provides in house opportunity for faculty to gain hands-on experience by practically doing experiments in the laboratories of the parent departments. The programme is being implemented in all the affiliated colleges of JNTU K to help the faculty to review and broaden their understanding of the practical aspects of the theoretical knowledge imparted by them to the students.

Objectives and Benefits

1. To mobilize and motivate the faculty to get familiarity with all the experiments of the apparatus, machinery, equipment, set up and facilities available in each laboratory of the parent departments
2. To broaden the understandingof the link between the theory and practice by making the faculty to do experiments
3. To help build the capacity of the faculty such that they can handle the laboratories of not only their specialization but also other specializations in the same department.
4. To serve indirect purpose of checking the working condition and maintenance of the apparatus, machinery, equipment, set up and facilities in the laboratories.
5. Weightage will be given in the ratifications to the faculty participating in this programme
6. Benefit to the student in instructions of relevance, importance and appreciation of experiments delivered by teachers.

The Organization

1. The Directorate of Faculty Development, JNTU K will organize, supervise and co-ordinate the programme " **Hands-on Experience for Faculty in Laboratories**" Phase I
2. All the I Semester Laboratories of 21 Departments are covered in the programme in Phase I as per details given in **Annexure 1**. The II Semester Laboratories will be covered in Phase II.
3. The programme is conducted in the departmental laboratories in all the affiliated colleges
4. The reporting mechanism, communication and the ownership will be as noted below



The implementation

1. It is mandatory for all the faculty teachingUG courses in all affiliated colleges of JNTUK to participate in the programme(The Principal and HOD's are exempted as they have to monitor the programme)
2. The laboratories of 21 departments given in **Annexure 1**, are included in the programme.
3. The faculty will conduct all the possible experiments according to R13 and R10 syllabi, on the apparatus, machinery, equipment, set up and facilities available in each laboratory of their departments.
4. The Heads of the Departments (HOD's) need to create awareness about the importance of the programme among the faculty members of their departments and encourage them to participate in the programme
5. The HOD's take lead to create necessary environment and make required arrangements in the department to implement the programme.
6. The Principal shall send the list of faculty who have not participated in the programme, along with the explanations for non-compliance

The Duration of Programme and Report Submission

1. The "**Hands-on Experience**" programme shall be conducted and completed in all aspects from 1.5.2014 to 30.6.2014.
2. **Conduct of Experiments** :The faculty will conduct the experiments using observation note books. They shall record their observations, draw the graphs, and write all the relevant details in the observation note books. These shall be maintained for each lab separately and kept in the departments for inspection and verification by authorities of the University.
3. **Submission of Report** :The faculty will prepare report for each labon hard copy for submission to the University. The report shall be prepared as per the format enclosed on A4 size sheet. **The report for a lab with 10 experiments will have 11 papers(Cover page + 10 papers for ten experiments)**
4. The HOD's will collect the reports from faculty and submit them to The Principal. The Principal will in turn submit the reports to The Director (Faculty Development), JNTUK, Kakinada on or before 7.7.2014

The Queries

1. The queries can be sent to abbaiah@yahoo.com with the subject name of **Hands- on Experience-Query** for any clarifications
2. The queries will also be answered on calling **0884 2355677**

Name of Experiment	PN JUNCTION DIODE CHARACTERISTICS
Importance of Experiment	a) To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode. b) To calculate the cut-in voltage at which diode conducts. c) To calculate static and dynamic resistance.
Apparatus Required	PN JUNCTION Diode IN4007. Regulated Power supply (0-30V) Resistor 470Ω Ammeters (0-100 mA, 0-500μA) Voltmeter (0-20V) Bread board Connecting wires
Inference /Outcome	Forward and Reverse Bias characteristics of p-n diode. Determination of Cut-in voltage, Static Resistance in Forward Bias, Dynamic resistance in Forward Bias, Static Resistance in Reverse Bias, Dynamic resistance in Reverse Bias.
Correlation of experimental outcome with theoretical concept	**Theory:** A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage. When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers. **Procedure**: **Forward Bias**:- 1. Connections are made as per the circuit diagram. 2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode. 3. Switch on the power supply and increase the input voltage (supply voltage) in Steps. 4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage. 5. The readings of voltage and current are tabulated.

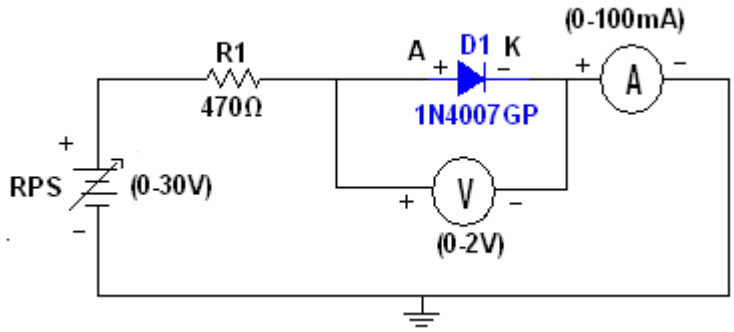
6. Graph is plotted between voltage and current.

7. Find the cut-in voltage in forward bias.

8. Now calculate the static and dynamic resistances.

Circuit Diagram:

Forward Bias:



Reverse Bias:

1. Connections are made as per the circuit diagram.

2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.

3. Switch on the power supply and increase the input voltage (supply voltage) in Steps.

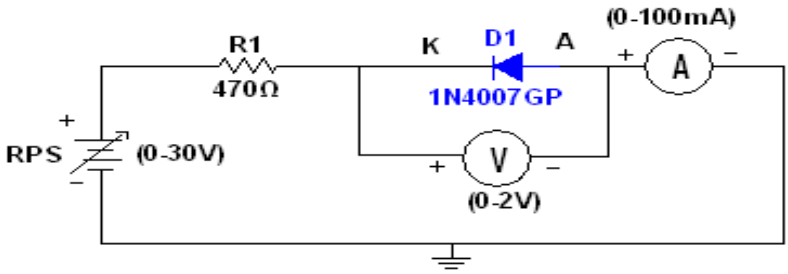
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated.

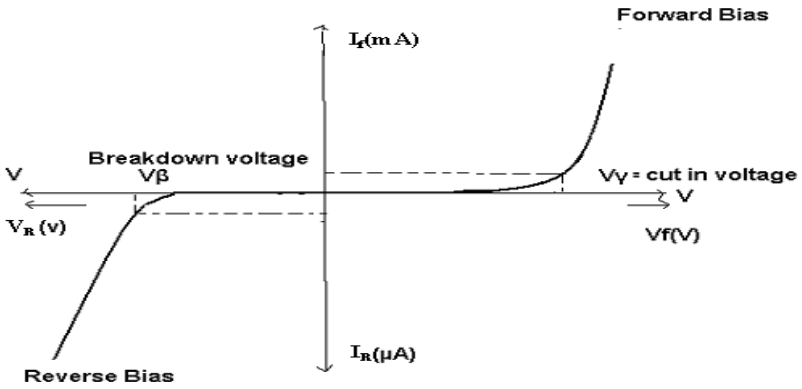
6. Graph is plotted between voltage and current.

7. Now calculate the dynamic resistance.

Reverse Bias:

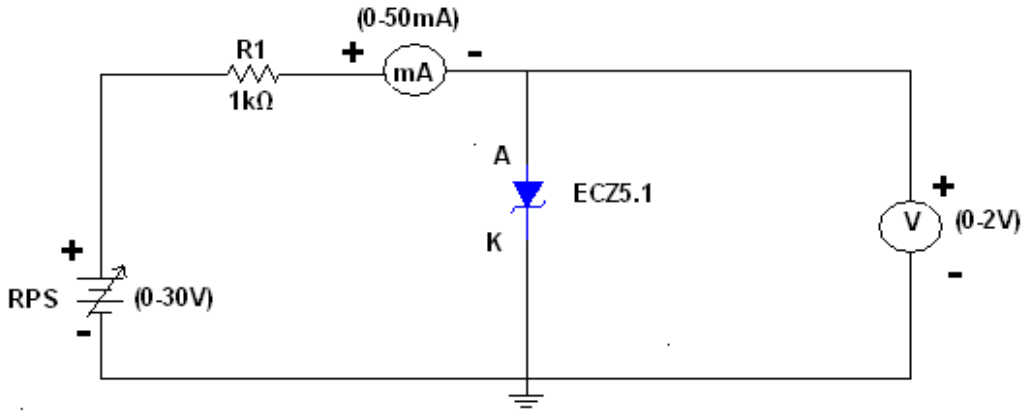
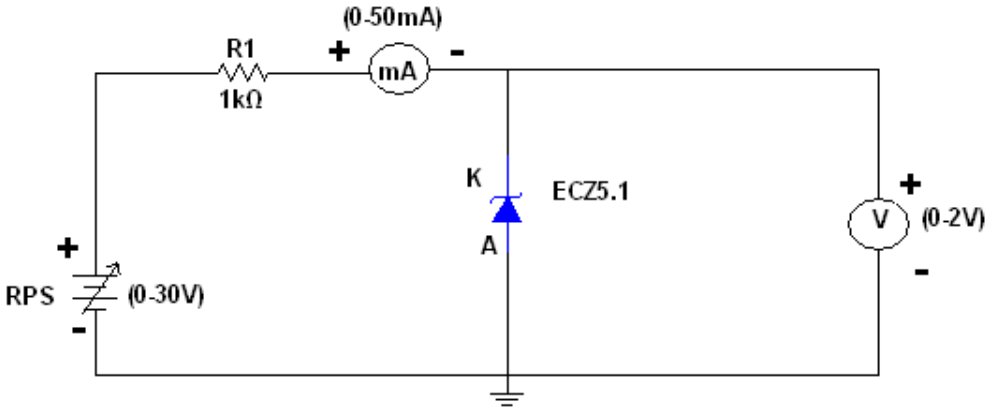


Parameter	Ideal/ Theoretical	Practical
Forward bias: Cut-in voltage of diode(Si)	0.7V	0.6V
Static Resistance:	low	$R_D = V_D/I_D$ 70Ω
Dynamic Resistance:	low	$r_d = \Delta V_d / \Delta I_d$ 10Ω
Reverse Bias: Static Resistance:	high	$R_D = V_D/I_D$ 40kΩ
Dynamic Resistance:	high	$r_d = \Delta V_d / \Delta I_d$

	Model Waveform: 
Practical Application	➢ As Rectifier in DC Power Supplies. ➢ In Demodulation or Detector Circuits. ➢ As DC Restorer in clamping networks. ➢ In clipping circuits used for waveform generation. ➢ As switches in digital logic circuits. ➢ Can be used as temperature measuring device. ➢ In over voltage protection circuits.
Can you design new experiment with this set up	Design an experiment to find the small signal components of PN junction diode.
Is the experimental set up in working condition	YES

Signature of Faculty Member

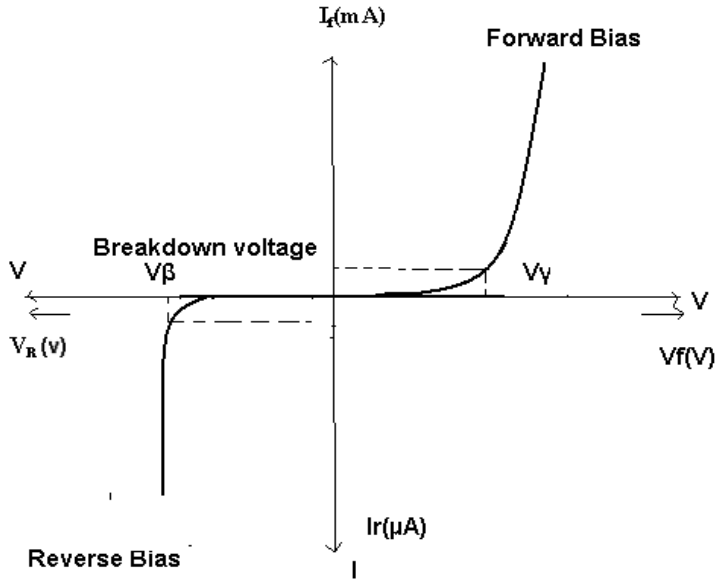
Name of Experiment	**ZENER DIODE CHARACTERISTICS AND ZENER AS A REGULATOR**
Importance of Experiment	a) To observe and draw the Forward and Reverse bias V-I Characteristics of a zener diode. b) To calculate the cut-in voltage at which diode conducts. c) To calculate static and dynamic resistance
Apparatus Required	Zener diode Z5.1 Regulated Power Supply- (0-30V). Voltmeter- (0-20V) Ammeter - (0-100mA) Resistor - 1KΩ Bread Board Connecting wires
Inference /Outcome	**Forward and Reverse Bias characteristics of Zener Diode** Determination of Cut-in voltage, Static Resistance in Forward Bias, Dynamic resistance in Forward Bias, Zener Break-down Voltage, Static Resistance in Reverse Bias, Dynamic resistance in Reverse Bias.

Correlation of experimental outcome with theoretical concept	A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But in zener diode if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators. **Circuit Diagram:** **Forward Bias:**  **Procedure:** **Forward Bias:** 1. Connections are made as per the circuit diagram. 2. The Regulated power supply voltage is increased in steps. 3. The zener current (Iz), and the zener voltage (Vz) are observed and then noted in the tabular form. 4. A graph is plotted between zener current (Iz) and zener voltage (Vz). 5. Find the cut-in voltage in forward bias. 6. Now calculate the static and dynamic resistances. **Reverse Bias**: 

Reverse Bias:

1. Connections are made as per the circuit diagram.
2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated.
6. Graph is plotted between voltage and current.
7. Find the breakdown voltage (knee voltage).
8. Now calculate the static and dynamic resistance

Model Waveforms:



	Ideal/ Theoretical	Practical
Cut-in voltage of diode(Si)	0.7V	0.75v
Static Resistance	low	$R_D = V_D/I_D$, 375Ω
Dynamic Resistance	low	$r_d = \Delta V_d / \Delta I_d$, 25Ω
Zener Break down voltage	5.1v	3v
Static Resistance	$R_D = V_D/I_D$	375 Ω
Dynamic Resistance	$r_d = \Delta V_d / \Delta I_d$	166.7Ω

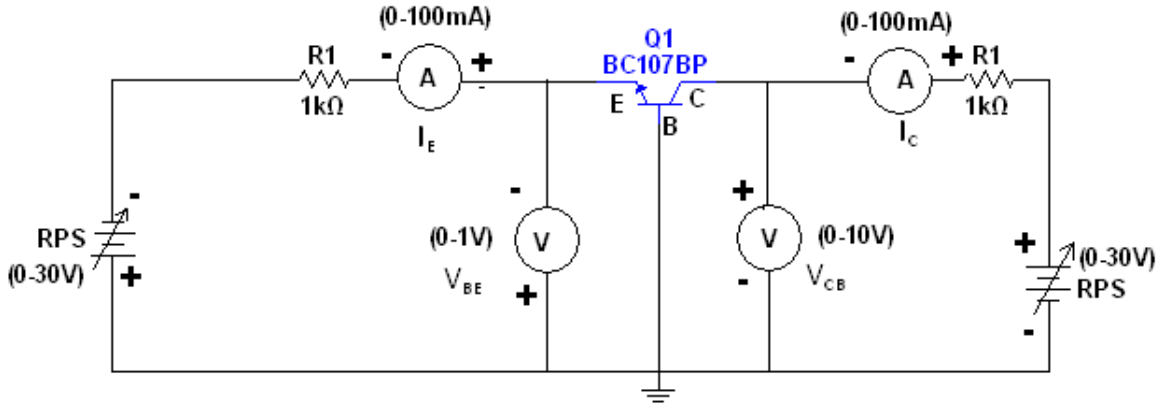
Practical Application

- Shunt Regulator
- Meter protection
- Peak clipper
- Switching operation
- Controlled comparator
- Power supplies

Can you design new experiment with this set up	Design an experiment to use zener diode as voltage regulator and obtain line and load regulation characteristics. Design an experiment to convert AC supply into DC supply.
Is the experimental set up in working condition	YES

Signature of Faculty Member

Name of Experiment	**TRANSISTOR CB CHARACTERISTICS**
Importance of Experiment	a) To observe and draw the input and output characteristics of a transistor connected in common base configuration. b) Calculate h-parameters from the characteristics
Apparatus Required	Transistor BC 107 Regulated power supply (0-30V) Voltmeter (0-20V) Ammeters (0-100mA) Resistor 1KΩ Bread board Connecting wires
Inference /Outcome	The input and output characteristics of the transistor in common Base configuration. Operating regions cut-off, active, saturation regions. H-parameters of transistor.
Correlation of experimental outcome with theoretical concept	A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased. It operates in three regions: active region, cut-off region and saturation region. Active region: When E-B junction is forward biased and C-B junction is reverse biased then the transistor is said to be in active region. Cut-off region: When E-B junction is reverse biased and C-B junction is reverse biased then the transistor is said to be in cut-off region. Saturation region: When E-B junction is forward biased and C-B junction is forward biased then the transistor is said to be in saturation region. In CB configuration, I_E is +ve, I_C is –ve and I_B is –ve. So, V_{EB}=f1 (V_{CB},I_E) and I_C=f2 (V_{CB},I_B) With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by, $\alpha = \Delta I_C / \Delta I_E$ **Circuit Diagram:**



Input Characteristics:

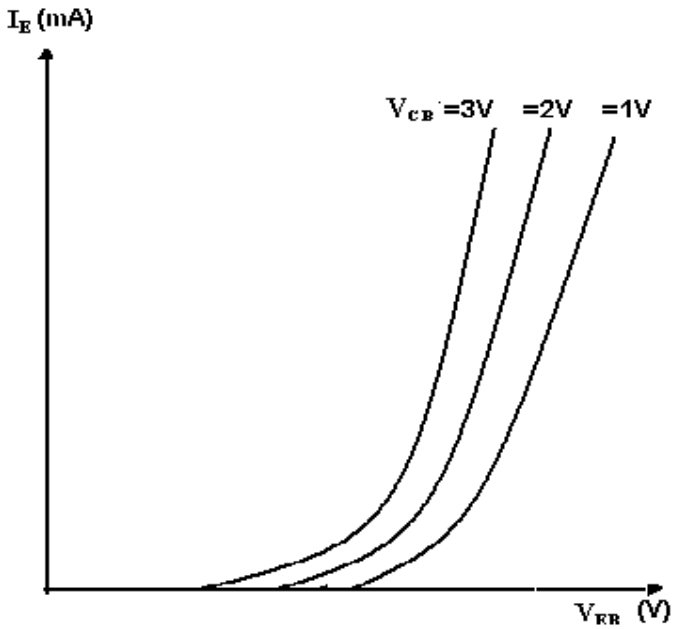
1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CB} is kept constant at 0V and for different values of V_{EB} note down the values of I_E.
3. Repeat the above step keeping V_{CB} at 1V, 2V, 4V and 6V and all the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant V_{CB}.

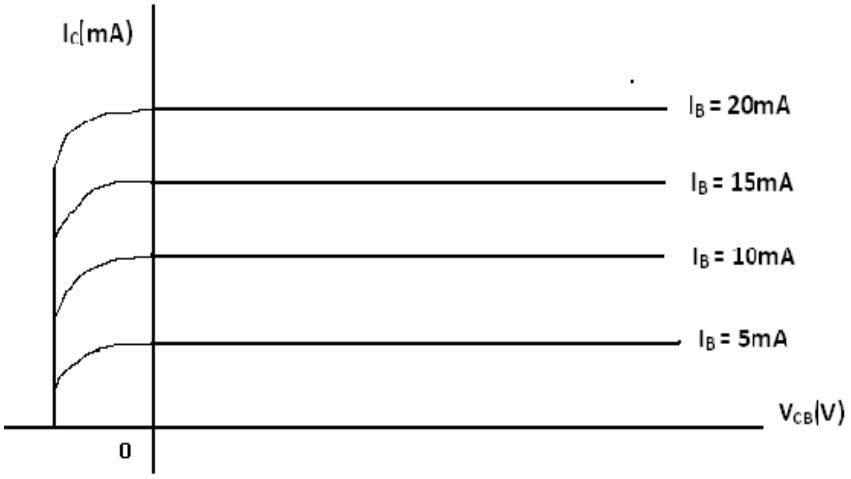
Output Characteristics:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input current I_E is kept constant at 10mA and for different values of V_{CB}, note down the values of I_C.
3. Repeat the above step for the values of I_E at 20mA, 40mA, and 60mA and all the readings are tabulated.
4. A graph is drawn between V_{CB} and Ic for constant I_E

Model Graphs:

Input Characteristics:



	Output Characteristics:  Input Impedance hib = $\Delta V_{BE} / \Delta I_E$ at V_{CB} constant=0.35 Output impedance hob = $\Delta V_{CB} / \Delta I_C$ at I_E constant=0.4 Reverse Transfer Voltage Gain hrb = $\Delta V_{BE} / \Delta V_{CB}$ at I_E constant=5mA Forward Transfer Current Gain hfb = $\Delta I_C / \Delta I_E$ at constant $V_{CB=}$1mA
Practical Application	➢ As a switch. ➢ As an amplifier. ➢ In oscillators. ➢ In power amplifiers.
Can you design new experiment with this set up	Design a circuit to use transistor as a switch in common base configuration. Determine the small signal model elements of transistor in common base configuration.
Is the experimental set up in working condition	YES

Signature of Faculty Member

Name of Experiment	**TRANSISTOR CE CHARACTERISTICS**
Importance of Experiment	a) To draw the input and output characteristics of transistor connected in CE configuration. b) To calculate h-parameters
Apparatus Required	Transistor (BC 107) R.P.S (0-30V) - 2Nos Voltmeters (0-20V) - 2Nos Ammeters (0-100mA, 0-200μA) Resistors 1KΩ Bread board
Inference /Outcome	The input and output characteristics of a transistor in CE configuration. Operating regions cut-off, active, saturation regions. H-parameters of transistor.
Correlation of experimental outcome with theoretical concept	**Theory:** A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with $V_{BE.}$ Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between I_c and V_{CE} at constant $I_{B.}$ The collector current varies with V_{CE} until few volts only. After this the collector current becomes almost constant, and independent of $V_{CE.}$ The value of V_{CE} upto which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to $I_{B.}$ It operates in three regions: active region, cut-off region and saturation region. <u>Active region:</u> When E-B junction is forward biased and C-B junction is reverse biased then the transistor is said to be in active region. <u>Cut-off region:</u> When E-B junction is reverse biased and C-B junction is reverse biased then the transistor is said to be in cut-off region. <u>Saturation region:</u> When E-B junction is forward biased and C-B junction is forward biased then the transistor is said to be in saturation region. The current amplification factor of CE configuration is given by $\beta = \Delta I_C / \Delta I_B$ **Procedure:-**

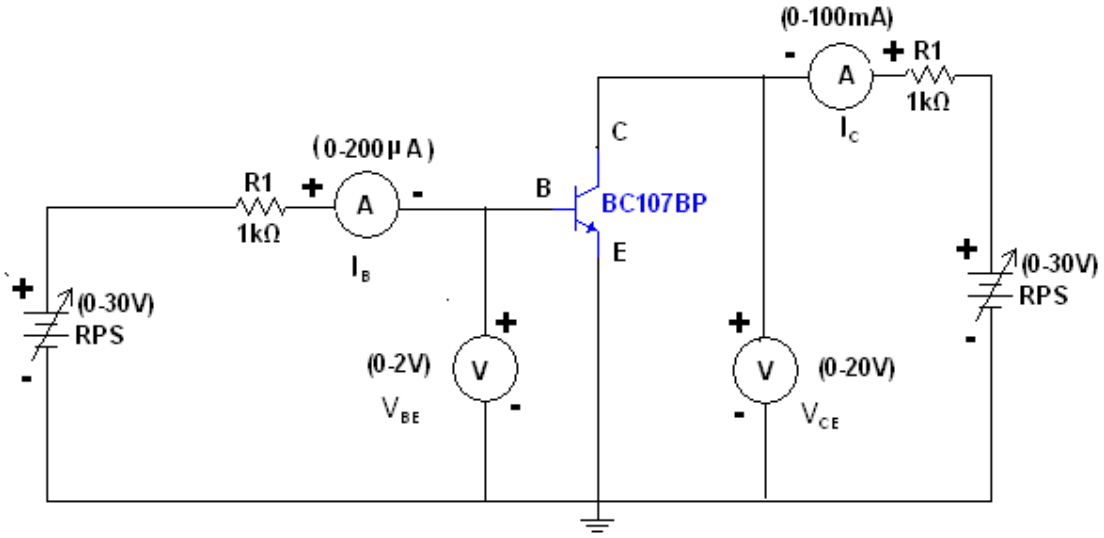
Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of $V_{BE.}$ Note down the values of I_C.
3. Repeat the above step by keeping $V_{CE\ at}$ 2V and 4V.
4. Tabulate all the readings.
5. Plot the graph between $V_{BE\ and}$ I_B for constant VCE.

Output Characteristics:

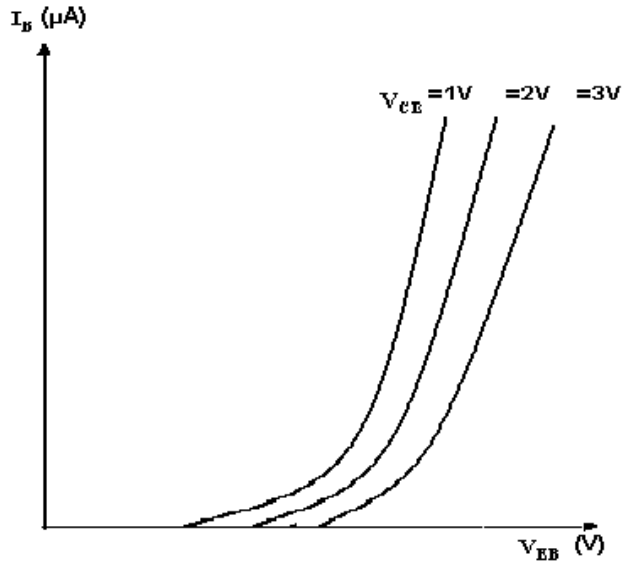
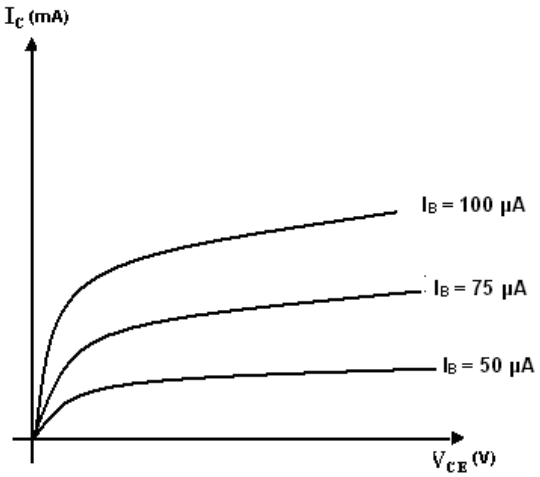
1. Connect the circuit as per the circuit diagram.
2. For plotting the output characteristics the input current IB is kept constant at 10µA and for different values of VCE, note down the values of I_C.
3. Repeat the above step by keeping I_B at 75 µA and 100 µA.
4. Tabulate the all the readings.
5. Plot the graph between V_{CE} and I_C for constant I_B.

Circuit Diagram:



Parameter	Ideal/ Theoretical	Practical
Cut in voltage(Si)	0.7	0.6
Input Impedance hie	HIGH	ΔV_{BE} / ΔI_B at V_{CE} constant
Output impedance hoe	LOW	ΔV_{CE} / ΔI_C at I_B constant
Reverse Transfer Voltage Gain hre	ΔV_{BE} / ΔV_{CE} at I_B constant	125
Forward Transfer Current Gain hfe	ΔI_C / ΔI_B at constant V_{CE}	8

Model Graphs:

	Input Characteristics:-  **Output Characteristics**:- 
Practical Application	➢ Acts as a switch ➢ As an amplifier ➢ As an inverter ➢ In oscillators
Can you design new experiment with this set up	Design a circuit to use transistor as a switch in common emitter configuration. Determine the small signal model elements of transistor in common emitter configuration.
Is the experimental set up in working condition	YES

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Name of Experiment	**RECTIFIER WITHOUT FILTERS (FULL WAVE & HALF WAVE)**
Importance of Experiment	a) To obtain the load regulation characteristics of rectifiers. b) To determine ripple factor and efficiency of rectifiers.
Apparatus Required	Bread Board Transformer (9-0-9) P-n Diodes (IN4007) - 2 No's Multimeters 2No's Connecting Wires Load resistor 1KΩ Decade Resistance Box 1
Inference /Outcome	The Ripple factor for the Half-Wave Rectifier and Full-Wave Rectifier without filter. The % of regulation of the Half-Wave rectifier and Full-Wave Rectifier. The % of efficiency of the Half-Wave rectifier and Full-Wave Rectifier.
Correlation of experimental outcome with theoretical concept	**Theory:Half Wave Rectifier:** During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage. During negative half-cycle of the input voltage, the diode D1 is in reverse bias and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter. For practical circuits, transformer coupling is usually provided for two reasons. 1. The voltage can be stepped-up or stepped-down, as needed. 2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit. **Procedure:-** 1. Connections are made as per the circuit diagram. 2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input. 3. By the multimeter, measure the ac input voltage of the rectifier and dc voltage at the output of the rectifier. 4. Find the theoretical value of dc voltage by using the formula,

$Vdc=V_m/\pi$

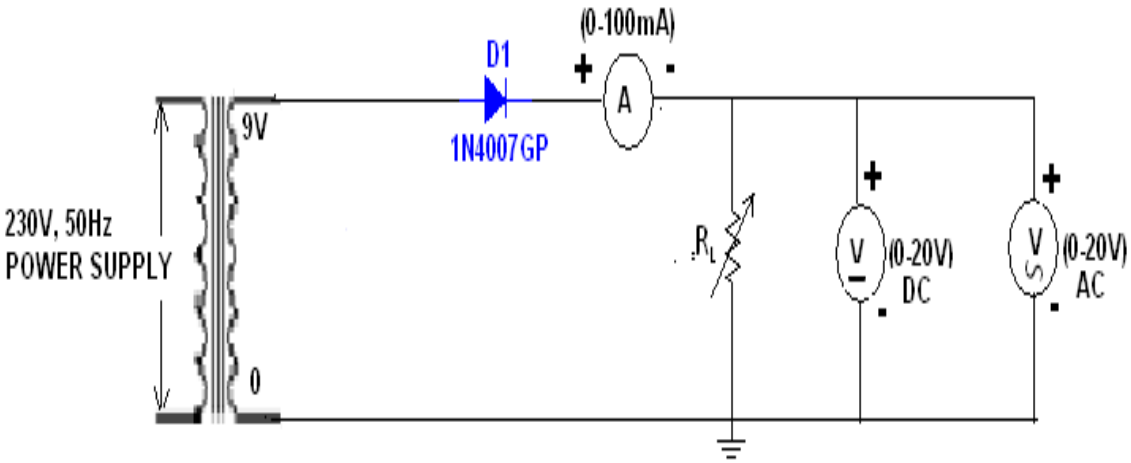
Where Vm= 2Vrms, (Vrms= output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage (Vrms)/dc output voltage (Vdc)

Circuit Diagram:

Without Filter:



Parameter	Ideal/ Theoretical	Practical
RMS Voltage	*Vrms=Vm/2*	Vm=10V Vrms=Vm/2=5V
DC or Average Volatge	*Vm/π*	*Vdc=Vm/π=3.184*
Ripple factor	*r=√ (Vrms/ Vdc) ^{2}*	*r=√ (Vrms/ Vdc) ^{2} -1 =1.21*
% Efficiency	*P_{dc}/P_{ac} *100* $P_{dc}= V_{dc}^2/R_L$ $P_{ac}= V_{rms}^2/R_L$ *P_{dc}/P_{ac} *100=40.8%*	$P_{dc}=$ $V_{dc}^2/R_L=0.0101$ $P_{ac}= V_{rms}^2/R_L=0.025$ *P_{dc}/P_{ac} *100=40.4%*

Full-Wave Rectifier: The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2 is reverse biased. The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph.

The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

Procedure:-

1. Connections are made as per the circuit diagram.

2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.

3. By the multimeter, measure the ac input voltage of the rectifier and dc voltage at the output of the

rectifier.

4. Find the theoretical value of dc voltage by using the formula,

$$Vdc=2Vm/\pi$$

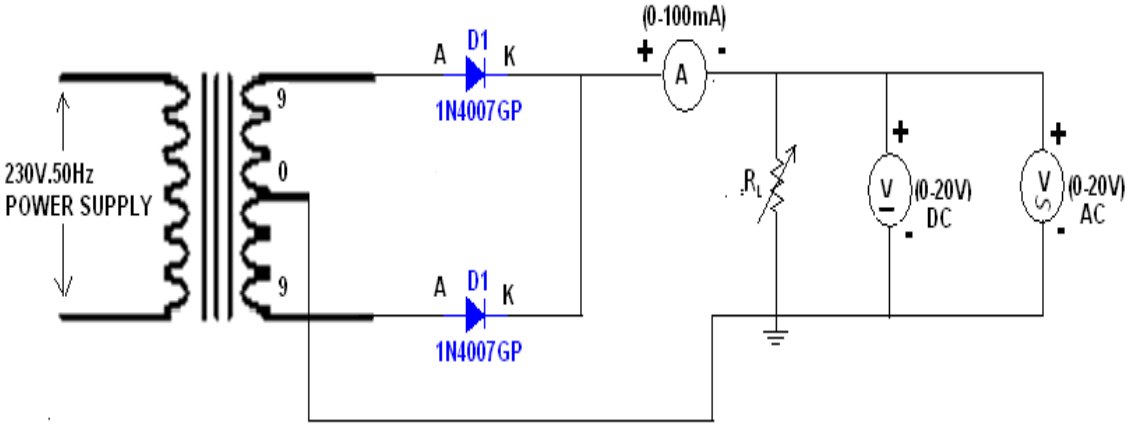
Where Vm= 2Vrms, (Vrms= output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage (Vrms)/dc output voltage (Vdc).

Circuit Diagram:-

With Out Filter:



Parameter	Ideal/ Theoretical	Practical
RMS Voltage	*Vrms=Vm/√2*	Vm=11V Vrms=7.77
DC or Average Volatge	*2* *Vm/π*	*Vdc=2Vm/π=7*
Ripple factor	*r=√ (Vrms/ Vdc) ^{2}*	*r=√ (Vrms/ Vdc) ^{2} -1 =0.481*
% Efficiency	*P_{dc}/P_{ac} *100* $P_{dc}= V_{dc}^2/R_L$ $P_{ac}= V_{rms}^2/R_L$ *P_{dc}/P_{ac} *100=80%*	$P_{dc}=$ $V_{dc}^2/R_L=0.0101$ $P_{ac}= V_{rms}^2/R_L=0.025$ *P_{dc}/P_{ac} *100=81.1%*

Practical Application	➢ *In Power Supplies* ➢ used for detection of amplitude modulated radio signals
Can you design new experiment with this set up	Design an experiment to achieve dc power supply and eliminate the ripples with inductor and capacitor filters.
Is the experimental set up in working condition	YES

Hands on Experience for Faculty in Laboratories
Phase I
JNTUK, Kakinada

Name of Experiment	**RECTIFIER WITH FILTERS (FULL WAVE & HALF WAVE)**
Importance of Experiment	a) To obtain the load regulation characteristics of rectifiers. b) To determine ripple factor and efficiency of rectifiers.
Apparatus Required	Bread Board Transformer (9-0-9) P-n Diodes (lN4007) - 2 No's Multimeters 2No's Connecting Wires Load resistor 1KΩ Decade Resistance Box 1 Capacitor (100μF/25v) – 1No
Inference /Outcome	The Ripple factor for the Half-Wave Rectifier and Full-Wave Rectifier with filter. The % of regulation of the Half-Wave rectifier and Full-Wave Rectifier. The % of efficiency of the Half-Wave rectifier and Full-Wave Rectifier.
Correlation of experimental outcome with theoretical concept	**Theory:** During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage. During negative half-cycle of the input voltage, the diode D1 is in reverse bias and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter. For practical circuits, transformer coupling is usually provided for two reasons. 1. The voltage can be stepped-up or stepped-down, as needed. 2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit. **HALF WAVE With filter:** **Procedure:-** 1. Connections are made as per the circuit diagram. 2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input. 3. By the multimeter, measure the ac input voltage of the rectifier and dc voltage at the output

of the rectifier.

4. Find the theoretical value of dc voltage by using the formula,

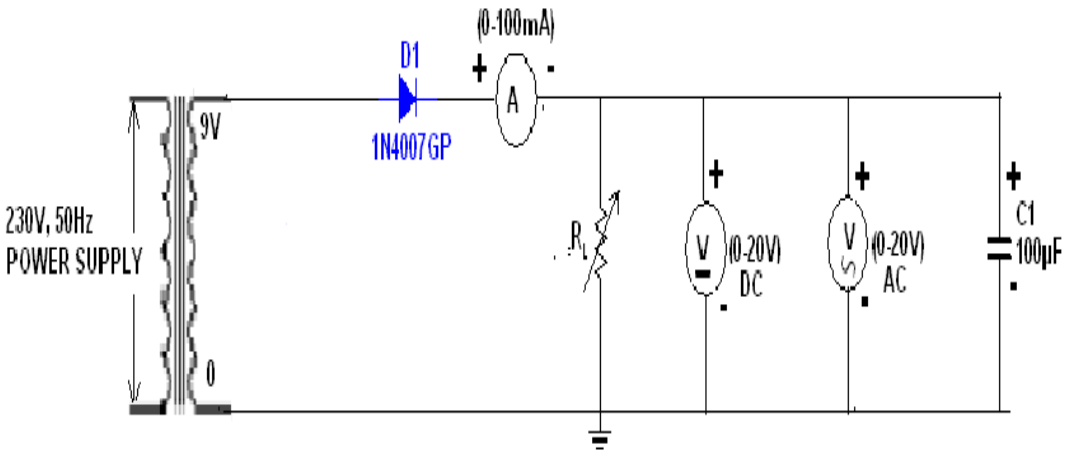
$$Vdc=V_m/\pi$$

Where Vm= 2Vrms, (Vrms= output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage (Vrms)/dc output voltage (Vdc)

circuit diagram:



Parameter	Ideal/ Theoretical	Practical
RMS Voltage	*Vrms=Vm/2*	Vm=10V Vrms=Vm/2=5V
DC or Average Volatge	*Vm/π*	*Vdc=Vm/π=3.184*
Ripple factor	*r=√ (Vrms/ Vdc) ^{2}*	*r=√ (Vrms/ Vdc) ^{2} -1 =1.21*
% Efficiency	*P_{dc}/P_{ac} *100* $P_{dc}= V_{dc}^2/R_L$ $P_{ac}= V_{rms}^2/R_L$ *P_{dc}/P_{ac} *100=40.8%* Ripple factor r=1/ (2√3 f C R) Where f =50Hz C =100µF R_L=1KΩ	$P_{dc}=$ V_{dc}^2/R_L=0.0101 $P_{ac}= V_{rms}^2/R_L$=0.025 *P_{dc}/P_{ac} *100=40.4%*
		0.057

FULL WAVE With Filter:
Procedure:-

1. Connections are made as per the circuit diagram.

2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.

3. By the multimeter, measure the ac input voltage of the rectifier and dc voltage at the output of the rectifier.

4. Find the theoretical value of dc voltage by using the formula,

$$Vdc=2Vm/\pi$$

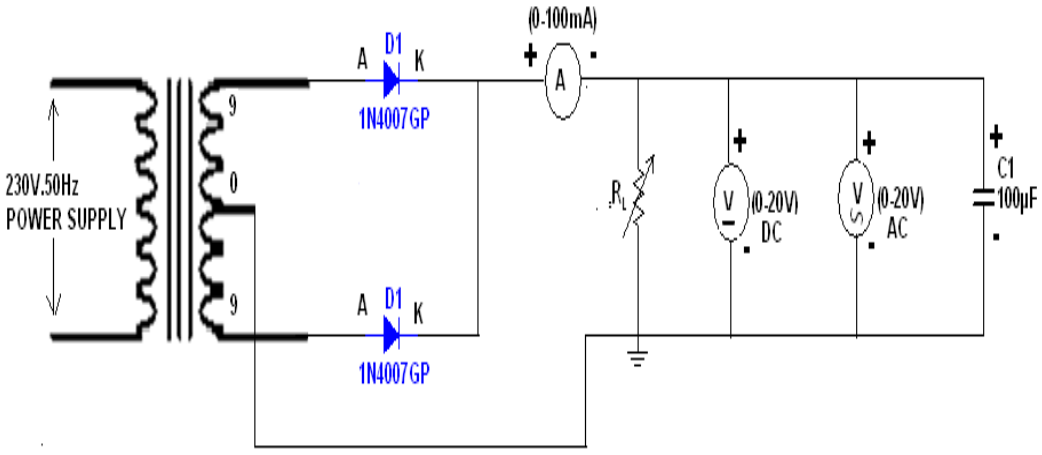
Where Vm= 2Vrms, (Vrms= output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage (Vrms)/dc output voltage (Vdc).

Parameter	Ideal/ Theoretical	Practical
RMS Voltage	*Vrms=Vm/√2*	Vm=11V Vrms=7.77
DC or Average Volatge	*2* *Vm/π*	*Vdc=2Vm/π=7*
Ripple factor	*r=√ (Vrms/ Vdc) ^{2}*	*r=√ (Vrms/ Vdc) ^{2} -1* *=0.481*
% Efficiency	*P_{dc}/P_{ac} *100* $P_{dc}= V_{dc}^2/R_L$ $P_{ac}= V_{rms}^2/R_L$ *P_{dc}/P_{ac} *100=80%* Ripple factor, r = 1/ (4√3 f C R_L) Where f =50Hz C =100µF R_L=1KΩ	$P_{dc}=$ V_{dc}^2/R_L=0.0101 $P_{ac}= V_{rms}^2/R_L$=0.025 *P_{dc}/P_{ac} *100=81.1%* 0.0114

circuit diagram:



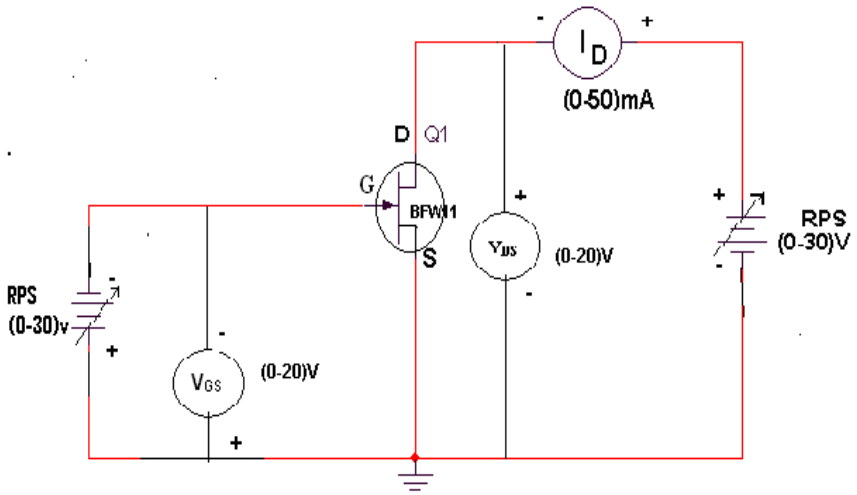
Practical Application	➢ Shunt Regulator ➢ Meter protection ➢ Peak clipper ➢ Switching operation ➢ Controlled comparator

	➢ Power supplies
Can you design new experiment with this set up	Design an experiment to achieve dc power supply and eliminate the ripples with inductor and capacitor filters.
Is the experimental set up in working condition	YES

Signature of Faculty Member

Name of Experiment	**FET CHARACTERISTICS**
Importance of Experiment	a) To draw the drain and transfer characteristics of a given FET b). to find the drain resistance (r_d) amplification factor (μ) and Transconductance (g_m) of the given FET.
Apparatus Required	FET (BFW-11) Regulated power supply (0-30)V Voltmeter (0-20V) Ammeter (0-100mA) Bread board Connecting wires
Inference /Outcome	The drain and transfer characteristics of a given FET. Determination of dynamic resistance (r_d), amplification factor (μ) and Tran conductance (g_m) of the given FET.
Correlation of experimental outcome with theoretical concept	A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage". If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage will be decreased. In amplifier application, the FET is always used in the region beyond the pinch-off. $F_{DS}=I_{DSS}(1-V_{GS}/V_P)\text{^}2$

Circuit Diagram:-



Procedure:-

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula

$$r_d = \Delta V_{DS}/\Delta I_D$$

11. From transfer characteristics, calculate the value of transconductace (g_m) By using the formula

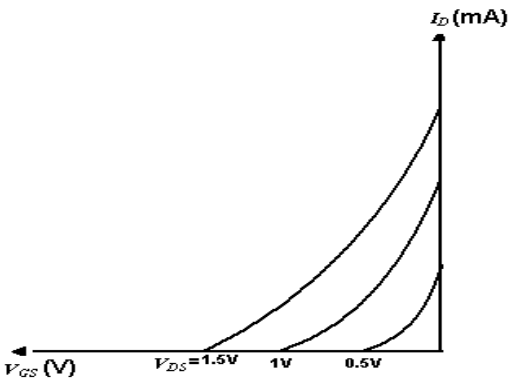
$$G_m = \Delta I_D/\Delta V_{DS}$$

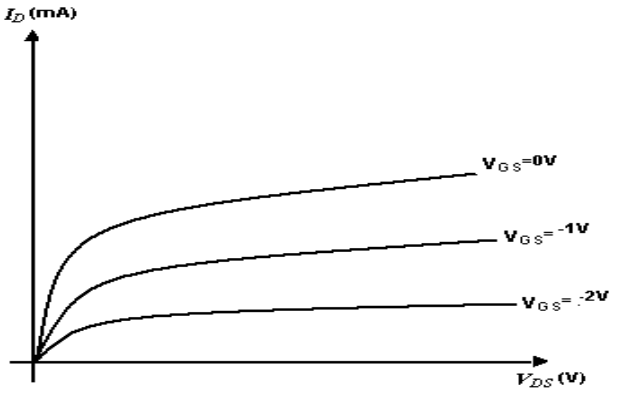
12. Amplification factor (μ) = dynamic resistance. Tran conductance

$$\mu = \Delta V_{DS}/\Delta V_{GS}$$

Model Graph:

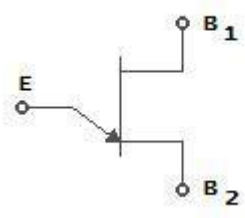
Transfer Characteristics



	Drain Characteristics  **Results:** Drain characteristics: Dynamic resistance(r_d)=$\Delta V_{DS}/\Delta I_D$ =1.14 Transfer Characteristics: Transconductance(g_m)= $\Delta V_{GS}/\Delta I_D$ = 3.5 Amplification Factor $\mu = g_{m*} r_d$ = 3.999
Practical Application	To use a FET as a temperature sensor in a practical application High Input Impedance Amplifier - Low-Noise Amplifier - Differential Amplifier - Constant Current Source - Analogue Switch or Gate - Voltage Controlled Resistor
Can you design new experiment with this set up	Determine the pinch off voltages for different gate to source voltages of given FET. Determine the relation between the small signal model components of given FET.
Is the experimental set up in working condition	Yes

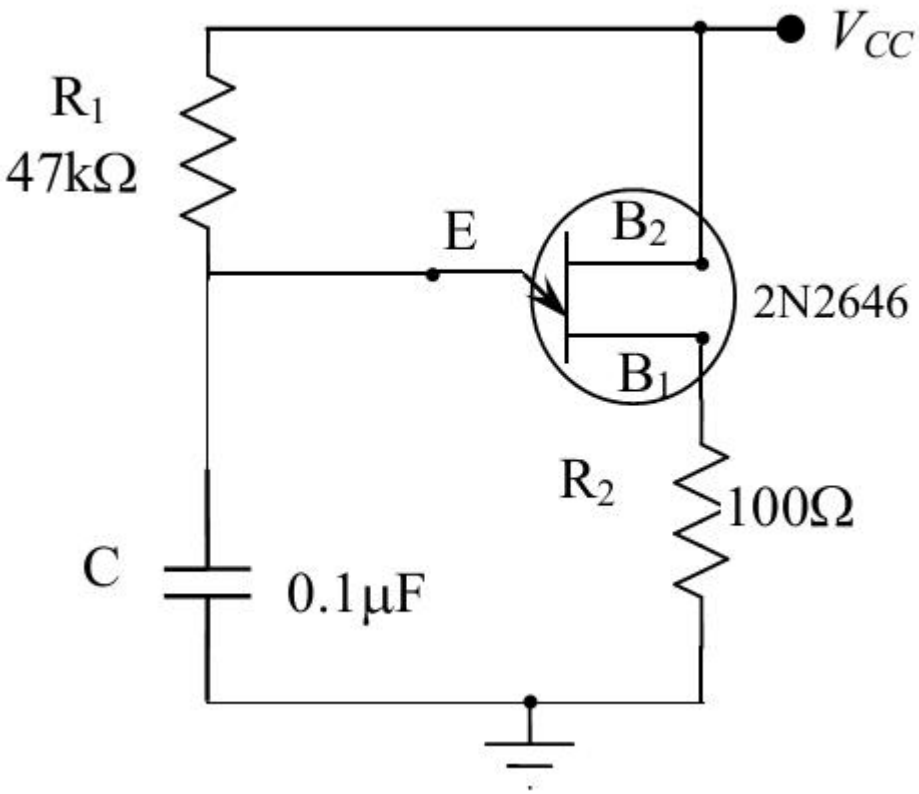
Signature of Faculty Member

Hands on Experience for Faculty in Laboratories
Phase I
JNTUK, Kakinada

Name of Experiment	**UJT CHARACTERISTICS**
Importance of Experiment	To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).
Apparatus Required	Regulated Power Supply (0-30V, 1A) - 2Nos UJT 2N2646 Resistors 10kΩ, 47Ω, 330Ω Multimeters - 2Nos Breadboard Connecting Wires
Inference /Outcome	To determine the characteristics of UJT and the value of Intrinsic Stand Off ratio
Correlation of experimental outcome with theoretical concept	A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.  The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven

approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.When the emitter voltage reaches V_p, the current startsto increase and the emitter voltage starts to decrease.This is represented by negative slope of the characteristics which is reffered to as the negative resistance region,beyond the valleypoint ,R_{B1} reaches minimum value and this region,V_{EB} propotional to $I_{E.}$

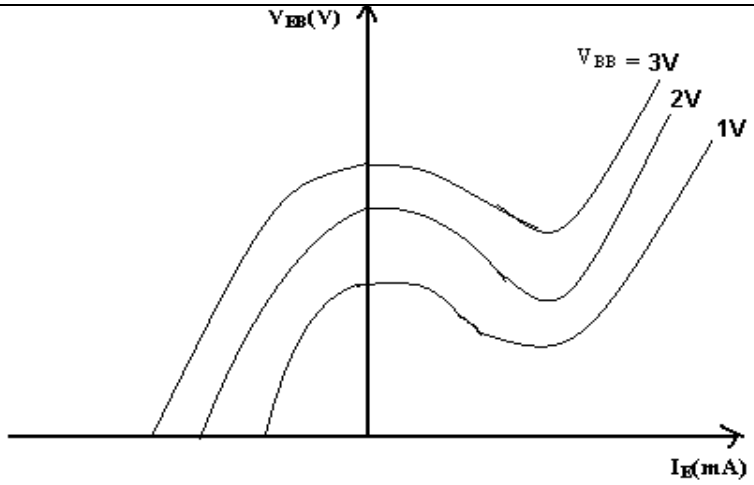
Circuit Diagram:



Procedure:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using $\eta = (V_p - V_D) / V_{BB}$
5. A graph is plotted between V_{EE} and I_E for different values of $V_{BE.}$

Model Graph:

	 **Result:** Intrinsic stand off ratio=0.0021
Practical Application	Relaxation Oscillator Triggering of SCR circuits
Can you design new experiment with this set up	yes
Is the experimental set up in working condition	yes

Signature of Faculty Member

Name of Experiment	**TRANSISTOR CE AMPLIFIER**
Importance of Experiment	To Measure the voltage gain of a CE amplifier To draw the frequency response of the CE amplifier To determine the Band width.
Apparatus Required	Transistor BC-107 Regulated power Supply (0-30V, 1A) Function Generator CRO Resistors [33KΩ, 3.3KΩ, 330Ω, 1.5KΩ 1KΩ, 2.2KΩ, 4.7KΩ] Capacitors 10μF -2No 100μF Bread Board Connecting Wires
Inference /Outcome	The voltage gain and frequency response of the CE amplifier. Band width of CE Amplifier.
Correlation of experimental outcome with theoretical	**Theory:** The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward

concept

biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

Procedure:

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 20mV peak-to-peak and 1 KHz frequency using Function Generator
3. Measure the Output Voltage Vo (p-p) for various load resistors
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression $A_v = (V_0/V_i)$
6. For plotting the frequency response the input voltage is kept Constant at 20mV peak-to-peak and the frequency is varied from 100Hz to 1MHz Using function generator
7. Note down the value of output voltage for each frequency.
8. All the readings are tabulated and voltage gain in dB is calculated by Using The expression $A_v = 20 \log_{10} (V_0/V_i)$
9. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis On Semi-log graph.

The band width of the amplifier is calculated from the graph Using the expression,

Bandwidth, $BW = f_2 - f_1$

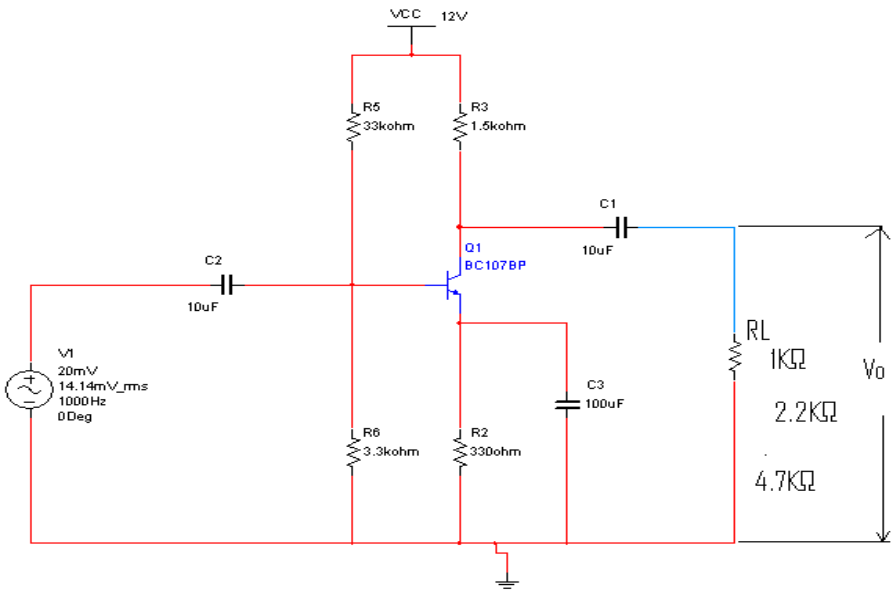
Where f_1 lower cut-off frequency of CE amplifier, and

Where f_2 upper cut-off frequency of CE amplifier

The bandwidth product of the amplifier is calculated using the Expression

Gain Bandwidth product=3-dBmidband gain X Bandwidth

Circuit Diagram:



Results:

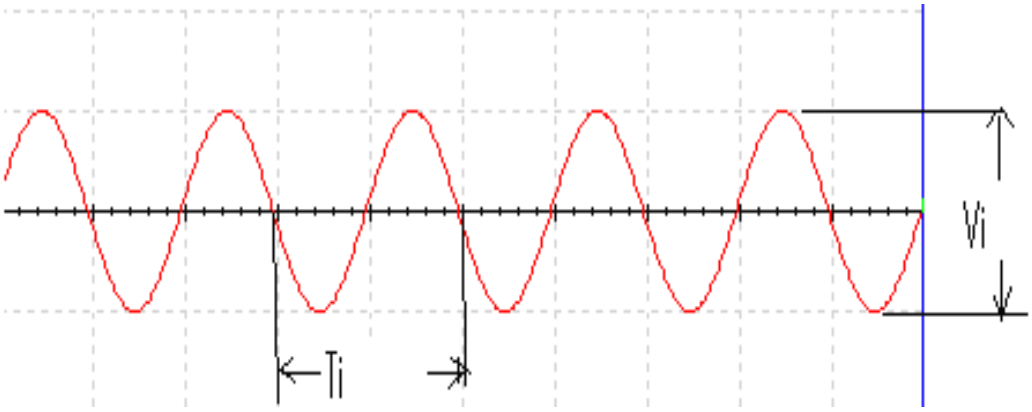
Lower cut off frequency=0.6k

Upper cut off frequency=350k

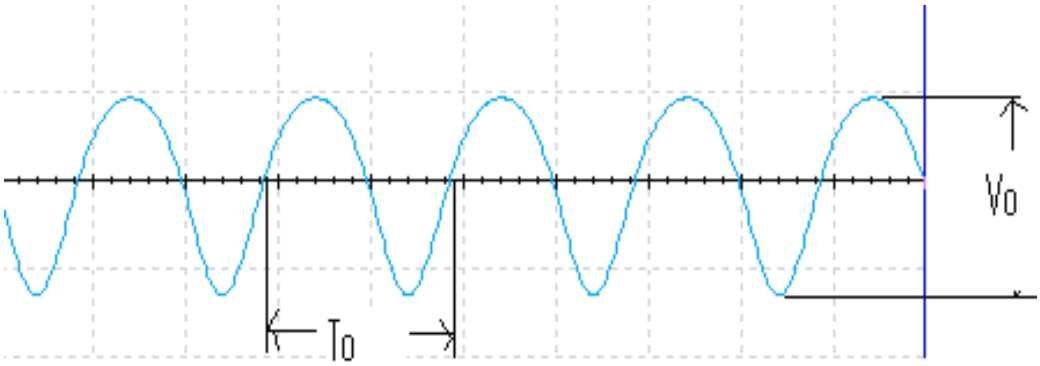
Bandwidth=349.4khz

Model wave Forms:

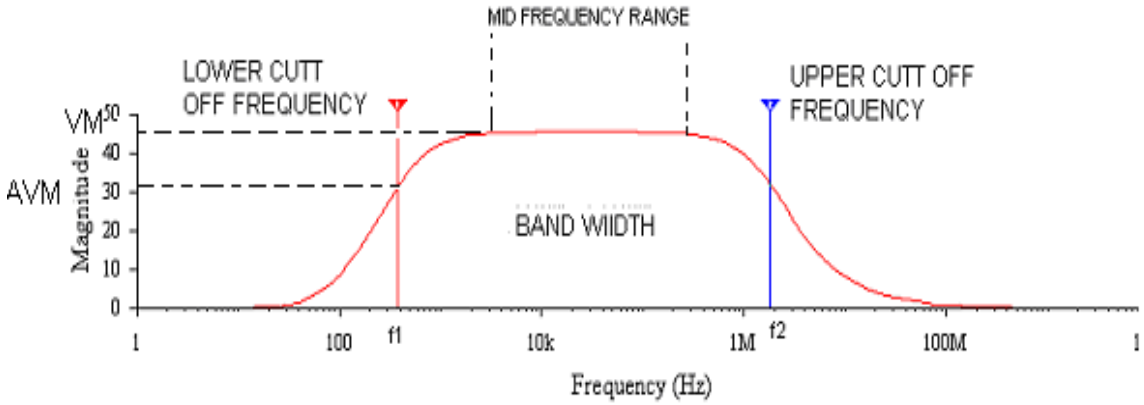
Input Wave Form:



Output Wave Form



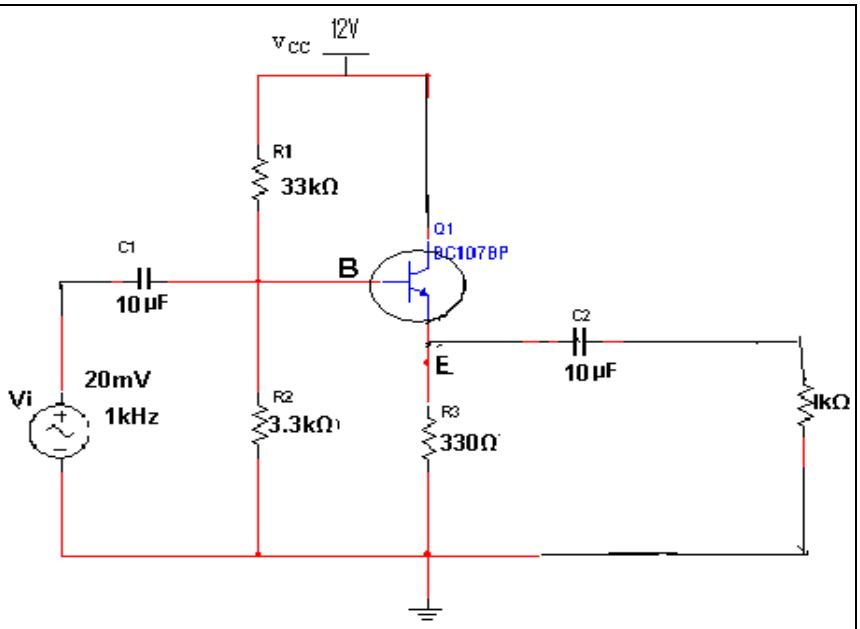
Frequency Response

	
Practical Application	Power amplifiers low frequency amplifiers voltage amplifiers radio frequency circuits It can used to design multistage amplifiers
Can you design new experiment with this set up	yes
Is the experimental set up in working condition	yes

Signature of Faculty Member

Name of Experiment	**COMMON COLLECTOR AMPLIFIER**
Importance of Experiment	To measure the voltage gain of a CC amplifier To draw the frequency response of the CC amplifier To find the Band width of CC Amplifier
Apparatus Required	Transistor BC 107 Regulated Power Supply (0-30V) Function Generator CRO Resistors 33KΩ, 3.3KΩ, 330Ω, 1.5KΩ, 1KΩ, 2.2KΩ & 4.7KΩ Capacitors 10µF -2Nos 100µF Breadboard Connecting wires

Inference /Outcome	The voltage gain and frequency response of the CC amplifier. Band width of CC Amplifier.
Correlation of experimental outcome with theoretical concept	**Theory:** In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation. This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower. **Procedure**: 1. Connections are made as per the circuit diagram. 2. For calculating the voltage gain the input voltage of 20mV peak-to-peak and 1 KHz frequency is applied and output voltage is taken for various load resistors. 3. The readings are tabulated. The voltage gain calculated by using the expression, $A_v=V_0/V_i$ 4. For plotting the frequency response the input voltage is kept constant a 20mV peak-to- peak and the frequency is varied from 100Hzto 1MHz. 5. Note down the values of output voltage for each frequency. All the readings are tabulated the voltage gain in dB is calculated by using the expression, $A_v=20\log 10(V0/V_i)$ 6. A graph is drawn by taking frequency on X-axis and gain in dB on y-axis on Semi-log graph sheet. The Bandwidth of the amplifier is calculated from the graph using the Expression, Bandwidth $BW=f_2-f_1$ Where f_1 is lower cut-off frequency of CE amplifier f_2 is upper cut-off frequency of CE amplifier 7. The gain Bandwidth product of the amplifier is calculated using the Expression, Gain -Bandwidth product=3-dB midband gain X Bandwidth **Circuit Diagram:**

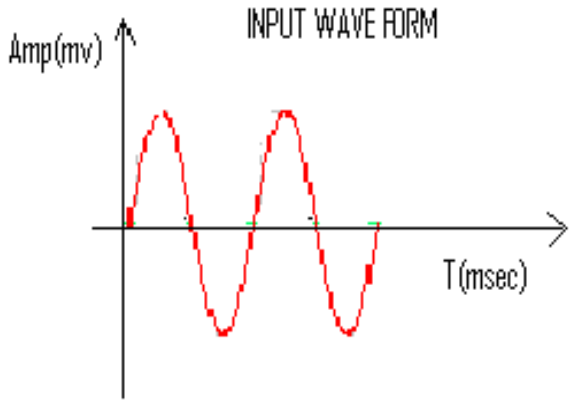


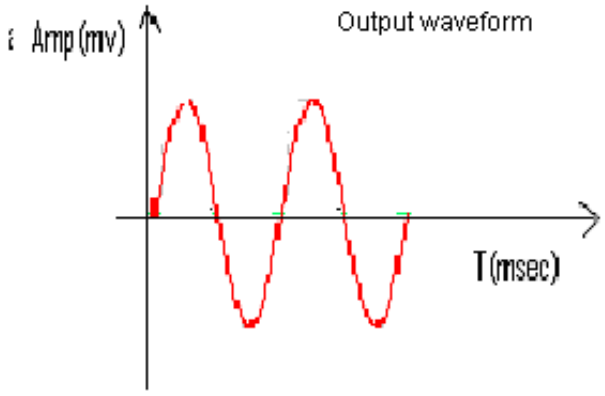
Results:

Voltage gain=1(theoretical), 0.99 (practical)

Bandwidth=f_2-f_1 = ∞

Waveforms:





Practical Application	It used as buffer Used for impedance matching

	used in the output stages of class-B and class-AB amplifiers
Can you design new experiment with this set up	yes
Is the experimental set up in working condition	yes

Signature of Faculty Member