LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY
An Autonomous Institution
Approved by AICTE & Permanently Affiliated to JNTUK, Kakinada
Accredited by NAAC with "A" Grade and NBA (CSE, EEE & ME)
Jonnada (Village), Denkada (Mandal), Vizianagaram Dist. – 535 005
Phone No. 08922-241111, 241112
E-Mail: lendi_2008@yahoo.com **Website: www.lendi.org**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech (Embedded Systems & VLSI Design) Course Structure –R19

(w.e.f the academic year 2019-20)

I Year -I Semester

S.No	Course Code	Subject Name	L	P	Credits
1	EC-ESVD1101	VLSI Technology	3	0	3
2	EC-ESVD1102	Embedded System Design	3	0	3
3	EC-ESVD1103	Digital Design Through Verilog	3	0	3
4	EC-ESVD1104	Programming Embedded System	3	0	3
5	EC-ESVD1105	**Program Elective-I**	3	0	3
	EC-ESVD1105.1	1. VLSI Digital Signal Processing systems			
	EC-ESVD1105.2	2. System-on-Chip design			
	EC-ESVD1105.3	3. Design For Testability			
6	EC-ESVD1106	**Program Elective -II**	3	0	3
	EC-ESVD1106.1	1. System design with Embedded Linux			
	EC-ESVD1106.2	2. Micro Electro Mechanical Systems (MEMS) Design			
	EC-ESVD1106.3	3. Digital signal processor and architecture			
7	EC-ESVD1107	Digital System Design Lab	0	4	2
8	AC-ERPW1101	**Audit Course 1:** English for Research Paper Writing	2	0	0
		Total	20	4	20

I Year –II Semester

S.No	Course Code	Subject Name	L	P	Credits
1	EC-ESVD1201	Analog IC Design	3	0	3
2	EC-ESVD1202	ASIC Design	3	0	3
3	EC-ESVD1203	Advanced Micro controls And Applications	3	0	3
4	EC-ESVD1204	Internet of things	3	0	3
5	EC-ESVD1205	**Program Elective**-III	3	0	3
	EC-ESVD1205.1	1. Communication Network Processors			
	EC-ESVD1205.2	2. Embedded Wireless Sensor Networks			
	EC-ESVD1205.3	3. Principles of Distributed Embedded Systems			
6	EC-ESVD1206	**Program Elective** -IV	3	0	3
	EC-ESVD1206	1. Memory technologies			
	EC-ESVD1206	2. Low power VLSI			
	EC-ESVD1206	3. CAD of digital systems			
7	EC-ESVD1207	Embedded system design lab	0	4	2
8	AC-RMIP1201	**Audit Course 2:** Research Methodology and IPR	2	0	0
		Total	**20**	**4**	**20**

II Year – I Semester

S.No	Course Code	Subject Name	L	P	Credits
1	EC-ESVD 2102	Seminar-I	0	0	02
2	EC-ESVD 2103	Project Stage-I	0	20	10
		Total	**0**	**16**	**12**

II Year – II Semester

S.No	Course Code	Subject Name	L	P	Credits
1	EC-ESVD2201	Project Stage-II	0	32	16
		Total	**0**	**32**	**16**

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC-ESVD1101	VLSI Technology	3	0	3

Course Objectives:

- To learn the basic MOS Circuits
- To learn the MOS Process Technology
- To understand the operation of MOS devices.
- To impart in-depth knowledge about Analog and digital CMOS circuits

Course Outcomes:

At the end of the course, the student will be able to

1. Understand the fabrication process of IC technology·.(L2)
2. Analysis of the physical design process of VLSI design flow.(L4)
3. Analysis of the design rules and layout diagram.(L4)
4. Design of Adders, Multipliers and memories etc.(L6).
5. Understand the floorplaning and chip design methodologies.(L2)

Unit I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor Processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC Designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the IC fabrication process.(L2)
- Outline the design rules and process parameters.(L2)
- Understand the design automation concepts..(L2)

Unit II

CMOS VLSI Design: MOS Technology and fabrication process of PMOS, NMOS, CMOS and BiCMOS technologies, comparison of different processes.

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, Communication interfaces, mixed signal interfaces.

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the C MOS technology fabrication process..(L2)
- Discuss the construction of building blocks in IC design.(L6)
- Outline the various design issues in IC fabrication.(L2)

Unit III

Basic electrical properties of MOS and Bi-CMOS circuits, MOS and Bi-CMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare MOS and Bi-MOS circuits.(L4)
- Discuss the qualitative and quantitative analysis.(L6)

Unit IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare switch logic and gate logic..(L4)
- Discuss the design procedure ALU subsystem.(L6)

Unit V

Floor Planning: Introduction, Floor planning methods, off-chip connections.
Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.
Chip Design: Introduction and design methodologies.
Learning Outcomes:
At the end of the unit, the student will be able to

- Compare various floor planning techniques and off-chip connections .(L4)
- Discuss the qualitative and quantitative analysis.(L6)

Text Books

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012.

Reference Books

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC-ESVD1102	Embedded System Design	3	0	3

Course Objectives

- To provide indepth knowledge about embedded processor, its hardware and software
- To explain programming concepts and embedded programming in C and assembly language
- To explain real time operating systems, inter-task communication and an embedded software development tool.

Course Outcomes:

At the end of the course, the student will be able to

1. To illustrate indepth knowledge about embedded processor, its hardware and software..(L2)
2. To explain programming concepts and embedded programming in C and assembly language..(L2)
3. To evaluate the performance serial and parallel buses that are used in system design,(L5)
4. To understand the Embedded System Design, Development, Implementation and Testing Embedded system design and development lifecycle model for creating an embedded system architecture,.(L2)
5. To design a Power PC Processor and Micro Blaze Processor based Embedded system design on Xilinx platform and also NiosII Processor based Embedded system design on Altera platform.(L6)

Unit I

Introduction an Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

Application: To design hardware for any of the Projects like Traffic Lights.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand embedded design flow and hardware design concepts..(L2)
- Outline to processor based embedded system design concepts.(L2)

Unit II

Embedded Hardware: Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance.

Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance.

Application: how to save data in different Memory devices like flip flop used in Frequency Divider.

Learning Outcomes:

At the end of the unit, the student will be able to

- Analyse embedded various building blocks and embedded processor.(L4)
- Discuss the embedded input/output devices working and applications.(L6)

Unit III

Embedded Software: Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples. Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

Application: implementing device drivers or transitions between protected modes of operation.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the device drivers for interrupt handling memory.(L2)
- Outline the various types of operating system are used programming the embedded system.(L2)

Unit IV

Embedded System Design, Development, Implementation and Testing Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design.
Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.
Application: Detect the Errors in any Embedded 'C' code
Learning Outcomes:
At the end of the unit, the student will be able to

- Understand the steps involved embedded product .(L2)
- Discuss issues in Hardware-Software design and co-design.(L6)
- Design the embedded system using CAD and laboratory tools .(L6)
- Explain the debugging tools are used in design a embedded product..(L2)

Unit V

Embedded System Design-Case Studies: Case studies- Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processor architectures should be taken into consideration while designing an Embedded System.
Application: Multi tasking Applications like mobile Software's.
Learning Outcomes:
At the end of the unit, the student will be able to

- Understand the steps involved Power PC Processor based system.(L2)
- Discuss issues in Xilinx platform-NiosII Processor based Embedded system.(L6)

Text Books

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier (Singapore) Pvt.Ltd. Publications, 2005.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

Reference Books

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.
4. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
5. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC-ESVD1103	Digital Design Through Verilog	3	0	3

Course Objectives:

- To learn the concepts of modelling a digital system using Verilog hardware description Language.
- Design digital circuits, behavioural and RTL modelling of digital circuits using Verilog HDL.
- Verify the modelling and synthesizing RTL models to standard cell libraries and FPGAs.
- Students gain practical experience by designing, modelling, implementing and verifying several digital circuits.

Course Outcomes:

At the end of the course, the student will be able to

1. Develop a model digital circuits using Verilog.(L6)
2. Understand the Function of any digital system using hardware description language.(L2)
3. Discuss Verilog hardware description languages (HDL).(L6)
4. Examine behavioural and RTL models. Describe standard cell libraries and FPGAs.(L3)
5. Develop a Synthesize RTL models to standard cell libraries and FPGAs. Implement RTL models on FPGAs and Testing & Verification.(L6)

Unit I

Basic Concepts – Verilog: Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modelling, Dataflow Modelling, Behavioural Modelling, Switch level modelling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench-lab exercise.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the steps involved Verilog HDL.(L2)
- Discuss issues Combinational UDP, Sequential UDP.(L6)

Unit II

Basics Of MOS Tranistors MOS Transistors- Threshold voltage- characteristics of MOS transistor channel length modulation- short channel effects- Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter- Power dissipation – Delay and sizing of inverters- Lab exercise.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the Threshold voltage and characteristics of MOS transistor channel length modulation.(L2)
- Analyze Power dissipation and Delay and sizing of inverters.(L4)

Unit III

CMOS – Combinational Circuits Static CMOS design-complementary CMOS - static properties-complementary CMOS design-Power consumption in CMOS logic gates dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic -Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection -Designing logic for reduced supply voltages. Lab exercise in Switch level modelling.

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare the static CMOS design-complementary CMOS and static properties.(L4)
- Design a logic for reduced supply voltages.(L6)

Unit IV

CMOS – Sequential Circuits Timing metrics for sequential circuit - latches Vs registers -static latches and registers – Bi-stability principle - multiplexer based latches-master slave edge triggered registers-non-ideal clock signals-low voltage static latches-static SR flip flop

Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bi-stable

sequential circuit-Schmitt trigger-mono stable -Astable -sequential circuit - choosing a clocking strategy. Lab exercise in Switch level modelling.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the Timing metrics for sequential circuit.(L2)
- Discuss issues in low voltage static latches and multiplexer based latches.(L6)
- Discuss issues in Xilinx platform-NiosII Processor based Embedded system.(L6)

Unit V

Sub-System Design/ System Verilog: addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines. Lab exercise.

Learning Outcomes:

At the end of the unit, the student will be able to

- Develop various CMOS circuits for addition and comparators etc.(L6)
- Discuss the importance of FSM in design of various types of systems.(L6)

Text Books

1. Samir palnitkar, ”Verilog HDL”, Pearson education, Second Edition,2003.
2. J. Bhasker, “A Verilog HDL Primer”, Second Edition, Star Galaxy, 2005.
3. J. Bhasker, “A Verilog Synthesis: A Practical Primer”, Star Galaxy, 1998
4. Jan.M.Rabaey., AnithaChandrakasanBorivoje Nikolic, "Digital Integrated Circuits", Second Editio
5. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition,Wesley, 1998.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1104	Programming Embedded System	3	0	3

Course Objectives:

- To make students familiar with the basic concepts and terminology of the target area, the embedded systems design flow.
- To give students an understanding of the embedded system architecture.
- To acquaint students with methods of executive device control and to give them opportunity to apply and test those methods in practice;
- To teach students to make measurements with the specified accuracy.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand basic concepts in the embedded computing systems area; (L2)
2. Determine the optimal composition and characteristics of an embedded system; (L5)
3. Design and program an embedded system at the basic level; (L6)
4. Understand the process of programming using c++ and JAVA for embedded system design(L2)
5. Develop hardware-software complex with the use of the National Instruments products.(L6)

Unit I

Introduction To Assembly Language and Data representation In C Assembly language programming – macros - Data representation – Twos complement, fixed point and floating point number formats – Low level programming in C: Primitive data types – Pointers – Structures – Unions – Dynamic memory allocation – Functions – recursive functions - Linked lists.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the Assembly language programming and macros .(L2)
- Discuss the Low level programming in C: Primitive data types, Pointers and Structures. (L6)

Unit II

Programming in C: Register usage conventions – Typical use of addressing options – Instruction sequencing – Procedure call and return – Functions – recursive functions -

Parameter passing – Retrieving parameters – Everything in pass by value – Temporary variables – threads – pre-emptive kernels – system timer – scheduling.

Learning Outcomes:

At the end of the unit, the student will be able to

- Develop various Register usage conventions based programs.(L6)
- Discuss the importance of Parameter passing and Retrieving parameters(L6)

Unit III

Object Oriented Programming: Object oriented analysis and design - C++ classes and objects – functions – data structures - examples. Object oriented analysis and design – JAVA classes and objects – functions – data structures - examples.

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare oriented programming programs C++, JAVA.(L4)
- Outline the classes and objects in JAVA programming(L2)

Unit IV

Unified Modeling Language: Connecting the object model with the use case model – Key strategies for object identification – UML basics. Object state behavior – UML state charts – Role of scenarios in the definition of behavior – Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the UML basics and state charts.(L2)
- Develop a model using UML concurrency design(L6)

Unit V

Embedded Software Development Tools and RTOS: The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS.

Learning Outcomes:

At the end of the course, the student will be able to

- Develop various C extensions for embedded systems.(L6)
- Discuss the system design using RTOS(L6)

References

1. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.
2. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education.
3. Steve Heath, “Embedded system design”, Elsevier, 2003.
4. David E. Simon, “An Embedded Software Primer”, Pearson Education, 2003.
5. E. Balaguruswamy, “Object oriented programming with C++”, Tata McGraw Hill, 2011.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1105.1	VLSI Digital Signal Processing Systems	3	0	3

Course Objectives:

- To Study the basic concepts and algorithms for dsp processor based systems
- To explain the folding transform and its importance,
- To elaborate the systolic Architectjure Design for develop a FIR based system
- To Discuss the importance of cook-Toom Algorithm in Fast convolution operation
- To Explain the power reduction techniques in processing DSP algorithms
- To discuss the applications and features of various DSP processor.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand the basic concepts and algorithms for dsp processor based systems(L2)
2. Discuss the folding transform and its importance,(L6)
3. Understand the systolic Architecture Design for develop a FIR based system(L2)
4. Discuss the power reduction techniques in processing DSP algorithms(L6)
5. Examine the applications and features of various DSP processor.(L4)

Unit I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms,

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming

Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the DSP algorithms benefits, Representation of DSP algorithms.(L2)
- DiscussPipelining of FIR Digital filters(L6)

Unit II

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the Folding Transform and- Register minimization Techniques.(L2)
- Apply a model Unfolding and Retiming (L3)

Unit III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the Systolic Array Design Methodology.(L2)
- Design a FIR filter for Space Representations contain Delays(L6)

Unit IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare Cook-Toom Algorithm and Winogard algorithm(L4)
- Understand the Low Power Design Scaling Vs Power Consumption.(L2)
- Analyze the power consumption in DSP systems and power reduction techniques(L4)

Unit V

Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing. Project based case studies.

Learning Outcomes:

At the end of the unit, the student will be able to

- Evaluate the programmable Digital Signal Processors .(L5)
- Discuss the applications of DSP techniques for Mobile and Wireless Communications(L6)

Text Books

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

Reference Books

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1105.2	System-on-Chip Design	3	0	3

Course Objectives:

- Understand the System Architecture and Processor Architecture, approach for a SOC Design.
- Learn the, Basic concepts in Processor Micro Architecture, and Learn Different Types of Processors like VLIW Processors, Superscalar Processors etc.
- Learn about SOC external memory, Scratchpads and Cache memory and Multilevel Caches.
- Learn the SOC Design approach, Design and evaluation, Applications Like Image compression etc.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand the SoC architecture and SoC design approach(L2)
2. Design of processor architectures like micro architecture, VLIW and super scalar architectures(L6)
3. Analyze performance of memory units like cache memory and memory requirements for SoC design(L4)
4. Design of Interconnect bus architectures in SoC design(L6)
5. Design of SoC for specific application like AES and JPEG compression(L6)

Unit I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing.System level interconnection, an approach for SOC Design, System Architecture and Complexity.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain the concept of system on chip (SoC) through standard design methodology(L2)
- Demonstrate the architectures of processor and components of the system(L2)

Unit II

Processors : Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Learning Outcomes:

At the end of the unit, the student will be able to

- Discuss the concepts in different processor architecture(L2)
- Explain different elements in instruction handling and its minimization(L2)

Unit III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memoryinteraction.

Learning Outcomes:

At the end of the unit, the student will be able to

- classify different types of memories(L2)
- outline the models of processor memory interaction(L2)

Unit IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor.

Learning Outcomes:

At the end of the unit, the student will be able to

- illustrate different bus architectures(L2)
- discuss bus transactions and contention time(L2)

Unit V

Interconnect Configuration: Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration – overhead analysis and trade-off analysis on reconfigurable Parallelism.

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Learning Outcomes:

At the end of the unit, the student will be able to

- Discuss different interconnect configurations(L2)
- Explain mapping design onto reconfigurable devices(L2)
- Analyze various design issues and techniques of SoC(L4)

Text Books

1. Computer System Design System-on-Chip – Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

Reference Books

1. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.
2. System on Chip Verification – Methodologies and Techniques – PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1105.3	Design for Testability	3	0	3

Course Objectives:

- Impart knowledge on the basic faults that occur in digital systems
- Describe fault detection techniques in combinational circuits.
- Outline procedures to generate test patterns for detecting single stuck faults in combinational and sequential circuits.
- Explain design for testability techniques with improved fault coverage.
- Introduce BIST concepts and specific architectures.
- Exposure to approaches for introducing BIST into logic circuits, memories and embedded cores.

Course Outcomes:

At the end of the course, the student will be able to

1. Design a Model digital circuits at logic and RTL levels (L6)
2. Evaluate digital ICs in the presence of faults and evaluate the given test set for fault coverage (L5)
3. Develop a test patterns for detecting single stuck faults in combinational and sequential circuits (L6)
4. Identify schemes for introducing testability into digital circuits with improved fault coverage(L3)
5. Compare different approaches for introducing BIST into logic circuits, memories and embedded cores (L4)

Unit I

Introduction to Test and Design for Testability (DFT) Fundamentals, Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of Modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain importance and challenges of VLSI Testing at different abstraction levels.(L2)
- Apply the concepts in testing which can help them design a better yield in IC design(L3)

Unit II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

Learning Outcomes:

At the end of the unit, the student will be able to

- Apply concepts of logic simulation and fault simulation in designing and testing of VLSI circuits.(L3)
- solve the problems associated with testing of semiconductor circuits at earlier design(L3)

Unit III

Testing for single stuck faults (SSF), Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models, Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

Learning Outcomes:

At the end of the unit, the student will be able to

- Apply various fault models for generation of test vectors.(L3)
- Identify the design for testability methods for combinational & sequential circuits(L4)

Unit IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and Observability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scans standards. Compression techniques – different techniques, syndrome test and signature analysis.

Learning Outcomes:

At the end of the unit, the student will be able to

- show a given circuit into a scan design.(L2)
- Analyze effect of logic built in self-test (a DFT technique) in VLSI circuits designing.(L4)

Unit V

Built-in self-test (BIST): BIST Concepts and test pattern generation.Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan

Learning Outcomes:

At the end of the unit, the student will be able to

- Apply various algorithms for test pattern generation.(L4)
- Identify the BIST techniques for improving testability.(L3)
- List the techniques to improve testability of a given circuit.(L4)

Text Books

1. MironAbramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch., Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.

References

1. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.
2. Bushnell, M., and Agrawal, Vishwani D, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers,2002

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1106.1	System Design with Embedded Linux	3	0	3

Course Objectives:

- To understand the fundamental parameters of a real time systems and difference to general operating system.
- To summarize the various functions of operating system and the changes needed for realtime operations.
- To analyse various realtime scheduling mechanisms and their performance in different conditions.
- To familiarize with task and its properties and task based communication methods.
- To impart with services and objects related to I/O, Timers and Interrupts etc.
- To understand the structure and functioning of various of practical real time operating systems.

Course Outcomes:

At the end of the course, the student will be able to

1. Outline the characteristic functions of real time systems.(L2)
2. Summarize the operating system functions and the characteristics changes of real time operating system.(L2)
3. Outline the task and its functions with different inter process communication techniques.(L2)
4. Analyze various realtime scheduling algorithms.(L4)
5. Outline the I/O, timer and interrupt specific objects and methods.(L2)

Unit I

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain the difference characteristics and constraining parameters of real time system.(L2)
- Summarize the processes and resources related to real time systems.(L2)

Unit II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Task States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use .

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare the operating system characteristics of general purpose operating system and real time operating system (L2).
- Explain the process management and process synchronization functions of real time operating systems.(L2)

Unit III

Approaches To Real Time Scheduling: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain various real time scheduling algorithms for real time operating systems.(L2)
- Analyze the working of different scheduling mechanisms with advantages and drawbacks.(L4)
- Compare scheduling methods of real time to the general purpose operating systems.(L4)

Unit IV

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

Learning Outcomes:

At the end of the unit, the student will be able to

- Summarize various methods in handling input and output operations of real time operating system.(L2)
- List various services and structures related in handling I/O subsystem of RTOS.(L1)

Unit V

Exceptions, Interrupts And Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Learning Outcomes:

At the end of the unit, the student will be able to

- Outline the handling of timers and their services in RTOS.(L2)
- Interpret the function and utilization of exceptions and interrupts in a RTOS.(L2)

Text Books

1. Richard Stevens, "Advanced Unix Programming".
2. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
3. Jane W.S. Liu, "Real Time Systems", Pearson Education.
4. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.

References

1. C.M.Krishna, KANG G. Shin, "Real Time Systems", McGraw.Hill
2. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
3. VxWorks Programmers Guide

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1106.2	Micro Electro Mechanical Systems (MEMS) Design	3	0	3

Course Objectives:

- To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices.
- To educate on the rudiments of micro fabrication techniques.
- To introduce various sensors and actuators
- To introduce different materials used for MEMS To educate on the applications of MEMS to disciplines beyond electrical and mechanical engineering.

Course Outcomes:

At the end of the course, the student will be able to

- Explain electrical and mechanical principles of MEMS (L2)
- Describe working of electrostatic, thermal and magnetic sensors and actuators (L2)
- Demonstrate piezoelectric effect and its applications (L2)
- Categorize micromachining processes (L4)
- Describe operation of polymer and optical MEMS (L2)

Unit I

Introduction : Intrinsic Characteristics Of MEMS – Energy Domains And Transducers- Sensors And Actuators – Introduction To Micro Fabrication – Silicon Based MEMS Processes – New Materials – Review Of Electrical And Mechanical Concepts In MEMS – Semiconductor Devices – Stress And Strain Analysis – Flexural Beam Bending- Torsional Deflection.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain basic principles of MEMS (L2)
- Classify materials used for fabricating MEMS (L4)
- Analyze stress, strain, bending and deflection in semiconductor devices (L4)

Unit II

Sensors and Actuators-I: Electrostatic Sensors – Parallel Plate Capacitors – Applications – Interdigitated Finger Capacitor – Comb Drive Devices – Micro Grippers – Micro Motors – Thermal Sensing And Actuation – Thermal Expansion – Thermal Couples – Thermal Resistors – Thermal Bimorph – Applications – Magnetic Actuators – Micromagnetic Components – Case Studies Of MEMS In Magnetic Actuators- Actuation Using Shape Memory Alloys.

Learning Outcomes:

At the end of the unit, the student will be able to

- Summarize different types of capacitor sensors (L2)
- Understand working of different thermal sensors (L2)
- Demonstrate the application of magnetic actuators (L2)

Unit III

Sensors and Actuators-II: Piezoresistive Sensors – Piezoresistive Sensor Materials – Stress Analysis Of Mechanical Elements – Applications To Inertia, Pressure, Tactile And Flow Sensors – Piezoelectric Sensors And Actuators – Piezoelectric Effects – Piezoelectric Materials – Applications To Inertia , Acoustic, Tactile And Flow Sensors.

Learning Outcomes:

At the end of the unit, the student will be able to

- Analyze piezoelectric effect and related mathematical concepts (L4)
- Demonstrate the applications of PZTs (L2)

Unit IV

Micromachining: Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching Of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case Studies – Basic Surface Micro Machining Processes – Structural And Sacrificial Materials – Acceleration Of Sacrificial Etch – Striction And Antistriction Methods – LIGA Process – Assembly Of 3D MEMS – Foundry Process.

Learning Outcomes:

At the end of the unit, the student will be able to

- Classify the types of etching processes applicable to micromachining (L4)

- Understand surface micromachining processes (L2)
- Describe various steps in LIGA process (L2)

Unit V

Polymer and Optical MEMS: Polymers In MEMS– Polimide – SU-8 – Liquid Crystal Polymer (LCP) – PDMS – PMMA – Parylene – Fluorocarbon – Application To Acceleration, Pressure, Flow And Tactile Sensors- Optical MEMS – Lenses And Mirrors – Actuators For Active Optical MEMS.

Learning Outcomes:

At the end of the unit, the student will be able to

- Discuss application of polymer materials in fabricating MEMS (L5)
- Describe operation of lenses, mirrors and actuators for optical MEMS (L2)

Text Books

1. Chang Liu, 'Foundations Of MEMS', Pearson Education Inc., 2012.
2. Stephen D Senturia, 'Microsystem Design', Springer Publication, 2000.
3. Tai Ran Hsu, "MEMS & Micro Systems Design And Manufacture" Tata McGraw Hill, New Delhi, 2002.

References

1. Nadim Maluf," An Introduction To Micro Electro Mechanical System Design", Artech House, 2000.
2. Mohamed Gad-El-Hak, Editor, " The MEMS Handbook", CRC Press Baco Raton, 2001.
3. Julian W. Gardner, Vijay K. Varadan, Osama O.Awadelkarim, Micro Sensors MEMS And Smart Devices, John Wiley & Son LTD, 2002.
4. James J.Allen, Micro Electro Mechanical System Design, CRC Press Publisher, 2005.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1106.3	Digital Signal Processors and Architecture	3	0	3

Course Objectives:

- To recall digital transform techniques.
- To introduce architectural features of programmable DSP Processors of TI and Analog Devices.
- To give practical examples of DSP Processor architectures for better understanding.
- To develop the programming knowledge using Instruction set of DSP Processors.
- To understand interfacing techniques to memory and I/O devices

Course Outcomes:

At the end of this course, students will be able to

- Identify and formalize architectural level characterization of P-DSP hardware
- Ability to design, programming (assembly and C), and testing code using Code Composer Studio environment
- Deployment of DSP hardware for Control, Audio and Video Signal processing applications
- Understand the major areas and challenges in DSP based embedded systems
- Analyze the FPGA based signal processing design using a case study of a complete design of DSP processor

Unit I

Programmable DSP Hardware: Processing Architectures (von Neumann, Harvard), DSP core algorithms (FIR, IIR, Convolution, Correlation, FFT), IEEE standard for Fixed and Floating Point Computations, Special Architectures Modules used in Digital Signal Processors (like MAC unit, Barrel shifters), On-Chip peripherals, DSP benchmarking.

Learning Outcomes:

At the end of the unit, the student will be able to

- Learn IEEE standard for Fixed and Floating Point Computations.
- Understand the basic of processing architecture and DSP core algorithms

Unit II:

Structural and Architectural Considerations: Parallelism in DSP processing, Texas Instruments TMS320 Digital Signal Processor Families, Fixed Point TI DSP Processors: TMS320C1X and TMS320C2X Family,TMS320C25 –Internal Architecture, Arithmetic and Logic Unit, Auxiliary Registers, Addressing Modes (Immediate, Direct and Indirect, Bit-reverse Addressing), Basics of TMS320C54x and C55x Families in respect of Architecture improvements and new applications fields, TMS320C5416 DSP Architecture, Memory Map, Interrupt System, Peripheral Devices, Illustrative Examples for assembly coding.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the TMS320C5416 DSP Architecture, Memory Map, Interrupt System, Peripheral Devices

Unit III

VLIW Architecture: Current DSP Architectures, GPUs as an alternative to DSP Processors, TMS320C6X Family, Addressing Modes, Replacement of MAC unit by ILP, Detailed study of ISA, Assembly Language Programming, Code Composer Studio, Mixed Cand Assembly Language programming, On-chip peripherals, Simple applications developments as an embedded environment.

Learning Outcomes:

At the end of the unit, the student will be able to

- Discuss about the TMS320C6X Family's Addressing Modes and MAC

Unit IV

Multi-core DSPs: Introduction to Multi-core computing and applicability for DSP hardware, Concept of threads, introduction to P-thread, mutex and similar concepts, heterogeneous and homogenous multi-core systems, Shared Memory parallel programming –OpenMP approach of parallel programming, PRAGMA directives, OpenMP Constructs for work sharing like for loop, sections, TI TMS320C6678 (Eight Core subsystem).

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand Multi-core computing and applicability for DSP hardware

Unit V

FPGA based DSP Systems: Limitations of P-DSPs, Requirements of Signal processing for Cognitive Radio (SDR), FPGA based signal processing design-case study of a complete design of DSP processor. High Performance Computing using P-DSP: Preliminaries of HPC, MPI, OpenMP, multicore DSP as HPC infrastructure.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the concepts of FPGA based signal processing design

Text Books

1. M. Sasikumar, D. Shikhare, Ravi Prakash, "Introduction to Parallel Processing", 1st Edition, PHI, 2006.
2. Fayez Gebali, "Algorithms and Parallel Computing",1st Edition, John Wiley & Sons, 2011
3. Rohit Chandra, Ramesh Menon, Leo Dagum, David Kohr, DrorMaydan, Jeff McDonald,"Parallel Programming in OpenMP", 1st Edition, Morgan Kaufman,2000
4. Ann Melnichuk,Long Talk, "Multicore Embedded systems", 1st Edition, CRC Press,2010.
5. Wayne Wolf, "High Performance Embedded Computing: Architectures, Applications and Methodologies", 1st Edition, Morgan Kaufman, 2006.
6. E.S.Gopi, "Algorithmic Collections for Digital Signal Processing Applications Using MATLAB", 1st Edition, Springer Netherlands, 2007.

I Year -I Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1107	Digital System Design Using HDL Lab	0	4	2

Course Objectives:

- To learn advanced digital design concepts.
- To design digital sub-systems using HDL.
- To learn Memory, CPLDs, FPGAs and ASICs.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand of Memory, CPLDs, FPGAs and ASICs
2. Interpret the HDL code as per the problem statement. (L2)
3. Analysis of digital circuits by Simulate the HDL code. (L3)
4. Implement the HDL code of the digital circuits in the FPGA.
5. Prepare the report of the experiment by HDL simulation and synthesis.

List Of Experiments:

1. Introduction to HDL Software and Hardware
2. Writing and Simulation of HDL programs for Half adder and Full adder
3. Writing, Simulation and Implementation of HDL programs for Multiplexer and Demultiplexer
4. Writing and Simulation HDL program for SM chart.
5. Writing, Simulation and Implementation of HDL program for given sequential circuit.
6. Writing, Simulation and Implementation of HDL program for Binary Multiplier.
7. BCD to Seven Segment Display Decoder
8. Traffic light controller using HDL.
9. Multi-Function Gate
10. Random Access Memory
11. Write HDL code to display messages on an alpha numeric LCD display
12. Implement Delay Flip flop using FPGA & CPLD.

I Year -I Semester

Code	Subject Name	L	T	P	C
AC-ERPW1101	English for Research Paper Writing	2	0	0	0

Course Objectives:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Course Outcomes:

At the end of the course, the student will be able to

1. Develop a writing skills by analyzing model texts (written by 'expert' writers) and texts written by students (with particular focus on issues involving coherence and cohesion);
2. Expand academic vocabulary;
3. Consolidate more advanced aspects of English grammar relevant to writing research papers;
4. Understand the language functions found in research papers;
5. Compare various practices and conventions used in writing research papers across a range of disciplines

Unit I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

Unit III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit IV

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

Unit V

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

Text books

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1201	Analog IC Design	3	0	3

Course Objectives:

- To educate that ICs are similar to discrete component circuits with special constraints.
- To expose to these constraints and make them design the ICs.
- To make them capable of arriving at a suitable architecture for a given function, realized in IC form.
- To compare and contrast Nyquist rate and over sampled DACs and ADCs

Course Outcomes:

At the end of the course, the student will be able to

1. Apply mathematics and physics to derive first order and second order MOSFET models (L3)
2. Analyze basic current mirror, Widlar and Wilson current mirror characteristics (L4)
3. Design simple CMOS amplifiers and analyze their performance (L6)
4. Estimate errors in a differential amplifier due to device mismatch (L6)
5. Discriminate between circuit verification and layout verification(L4)

Unit I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

Learning outcomes:

At the end of the unit, the student will be able to

- Relate resistors, capacitors, diodes and BJTs as MOS ICs (L2)
- Obtain first order and second order mathematical models for a MOSFET (L1)
- Illustrate basic CMOS amplifier configurations with different types of loads (L2)

Unit II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

Learning outcomes:

At the end of the unit, the student will be able to

- Distinguish between a MOSFET current source and a current sink (L4)
- Compare and contrast basic current mirror with Widlar and Wilson current mirrors (L2)
- Evaluate performance of Zener and Band gap references (L5)

Unit III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

Learning outcomes:

At the end of the unit, the student will be able to

- Analyze CS amplifier with different types of loads and compare their gain and Z_{out} (L4)
- Analyze performance of a CMOS cascade amplifier and their architectures (L4)
- Compare cascode and folded cascode amplifier performances (L2)

Unit IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

Learning outcomes:

At the end of the unit, the student will be able to

- Find gain, BW and phase characteristics of two and three stage CMOS OPAMPS (L1)
- Improve gain and output impedance of an OPAMP by cascade technique (L6)
- Suggest process and temperature independent compensation techniques for CMOS OPAMPs (L6).

Unit V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Practical Aspects and Design Verification: Semi-custom and cell library based design. Design of. Hardware description languages for high level design. Logic, circuit and layout verification. Analog Testing and Layout issues. Introduction to different tool used in Analog design.

Learning outcomes:

At the end of the unit, the student will be able to

- Design semi custom and cell library based analog circuits.(L6)
- Verify the simulations and layouts of different tools(L5)

Text Books

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1202	ASIC Design	3	0	3

Course Objectives:

- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures and interconnects.
- To comprehend the low power design techniques and methodologies.
- To learn the internal architecture, types and construction of ASICs

Course outcomes:

At the end of the course the student should be able to:

1. Discuss the concepts of ASIC design methodology, data path elements, operators, I/O cells. (L5)
2. Apply logical effort technique for predicting delay, delay minimization and FPGA architectures. (L3)
3. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow. (4)
4. Explain algorithms for floor planning and placement of cells for optimized area and speed.(L2)
5. Compare PSP,OTC,MCM systems.(L2).

Unit I

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.

Learning outcomes:

At the end of the unit, the student will be able to

- Explain the algorithms used for ASIC construction.(L2)
- Develop Full Custom Design Flow and Tools(L3)
- compare Semicustom Design Flow and Tool used - from RTL to GDS and Logical to Physical Implementation(L2)

Unit II

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages. Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.

Learning out comes:

At the end of the unit, the student will be able to

- Determine the issues involved in ASIC design, including technology choice, design management and tool-flow.
- Explain the algorithms used for ASIC construction with library design.

Unit III

Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. Low-level design entry: Schematic entry: Hierarchical design, Netlist screener. ASIC Construction: Physical Design, CAD Tools. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

Learning outcomes:

At the end of the unit, the student will be able to

- Design various programmable ASIC I/O cells and blocks.(L6)
- Construct ASIC physical designs using CAD TOOLS.(L6)

Unit IV

Floor planning Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.

Learning outcomes:

At the end of the unit, the student will be able to

- Full Custom Design Flow and Tool used.(L4)
- Explain goals and objective of placement algorithm.(L2)

Unit V

Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC.

Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

Learning outcomes:

At the end of the unit, the student will be able to

- Illustrate the concepts of PSP,OTC,MCM and PLAS.(L2)
- compare different arrays-gate matrix layout-1D and 2D compaction.(L4)

Text Books

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003

Reference Books

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations”, Springer, 2011, ISBN: 978-1-4614-1119-2. R4. Rakesh Chadha, Bhasker J., “An ASIC Low Power Primer”, Springer, ISBN: 978-1-4614-4270-7

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1203	Advanced Micro Controls and Applications	3	0	3

Course objectives:

- Introduce to arm architecture based microcontroller cortex M4.
- Show various instructions and working in different states of cortex M4 microcontrollers.
- Familiarize with various low power states and system control features of standard cortex M4 microcontroller.
- Visualize the working of floating point unit of cortex M4 microcontroller.
- Introduce to fault handling mechanism of cortex M4.
- Show the embedded development tools based on cortex M4.

Course outcomes:

At the end of the course, the student will be able to

1. Outline various architectural features of ARM cortex M4 based microcontroller with emphasis on memory, programming model and control functions of the system.(L2)
2. Demonstrate various instructions groups of ARM cortex M4 towards memory protection, low power operation, data conversion and their program design flow.(L3)
3. Illustrate the low power and system control features of cortex M4 series microcontroller with various timers, sleep modes and control registers for their low power design.(L2)
4. Interpret the working of the floating point unit designed with in the cortex M4.(L2)
5. Elaborate the features of ARM cortex with the fault handling capabilities based on the registers, detection and control of faults or exceptions.(L6)

Unit I

Introduction to ARM Cortex M Processors: What are ARM Cortex M Processors, advantages of the Cortex M Processors, applications of the ARM Cortex M processors ,Technical overview, general information, Architecture – introduction, programmer's model, behaviour of the application program status word, memory system, exceptions and interrupts, system control block, Debug.

Application: used in System on Chip used in SAMSUNG GALAXY S.

Learning outcomes:

At the end of the unit, the student will be able to

- Illustrate the concepts of ARM Cortex M Processors.(L2)
- Discuss the applications of the ARM Cortex M processors.(L4)

Unit II

Instruction set of ARM Cortex M4: moving data within the processor, memory access, arithmetic operations, logic operations, shift and rotate instructions, data conversion operations, bit field processing, compare and test, program flow control, saturation operations, exception related instructions, sleep mode-related instructions, memory barrier instructions.

Application: Used in Low power Consumption Applications like Mobiles and FPGA kits.

Learning outcomes:

At the end of the unit, the student will be able to

- Understand the concepts of Instruction set of ARM Cortex M4.(L2)
- Discuss the exception related instructions, sleep mode-related instructions, memory barrier instructions.(L4)

Unit III

Low power and system control features of ARM Cortex M4: Low power designs, low power features – sleep modes, system control register, entering sleep mode, wake-up conditions, sleepon-exit feature, SEVONPEND, sleep extension/wake-up delay, WIC, event communication interface, low power features using WFI &WFE instructions in programming.

Learning outcomes:

At the end of the unit, the student will be able to

- Illustrate the concepts of Low power and system control features of ARM Cortex M4.(L2)
- compare different types of mode of instructions.(L4)

Unit IV

Cortex M4 floating point unit: overview, floating point register overview, CPACR register, floating point register bank, FPSCR, FPCCR, FPCAR, FPDSCR, media and floating point feature registers.

Application: Floating point operation used in CPU.
Learning outcomes:
At the end of the unit, the student will be able to

- Outline the Cortex M4 floating point unit: overview.(L2)
- compare media and floating point feature registers.(L4)

Unit V

Fault exceptions & fault handling of ARM Cortex M4: causes of faults, enabling fault handlers, fault status registers and fault address registers, analyzing faults.
Application: Used in Mode view Controllers.
The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/ Decompiler, Simulators, Emulators and Debugging.
Application: identify the different types of files related to different groups.
Learning outcomes:
At the end of the unit, the student will be able to

- .Illustrate the concepts of the Embedded System Development Environment.(L2)
- Outline the Types of Files Generated on Cross-compilation.(L4)

References

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", Newnes, (Elsevier), 3rd Edition, 2014.
2. Shibu. K. V., "Introduction to Embedded Systems", Tata McGraw Hill Education Private Ltd., 2nd Edition, 2009.
3. David A Patterson, John L Hennessy, "Computer Organization and Design – ARM Edition", Morgan Kauffman Publishers Elsevier, 4th Edition, 2010.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1204	Internet of Things	3	0	3

Course Objectives:

- To present interconnection and integration of the physical world and the cyber space.
- To demonstrate applications of Internet of Things
- To educate building blocks and characteristics of Internet of Things
- To introduce communication protocols used in Internet of Things
- To impart knowledge on design & develop IoT devices

Course Outcomes:

At the end of the course, the student will be able to

1. Explain the structure and levels of abstraction of a IoT system with enabling technologies.(L2)
2. Examine the application areas of IoT with unique skills and challenges relevant to the domain. (L4)
3. Illustrate revolution of Internet in Mobile Devices, Cloud & Sensor Networks with emphasis on M2M communication.(L2)
4. Make use of python programming to implement Internet of Things. (L3)
5. Design IoT applications using Raspberry Pi (L3)

Unit I

Introduction & Concepts: Introduction to Internet of Things, physical design of IoT, logical design of IoT, IoT enabling Technologies, IoT levels.

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain different levels of IoT system and their needed prerequisites.(L2)
- Outline different technologies that enable IoT and its applications.(L2)

Unit II

Domain Specific IOTs: Home Automation, Cities, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health & Life Style.

Learning Outcomes:

At the end of the unit, the student will be able to

- To extend the understanding of IoT to different application domains.(L2)
- To relate the different fields of engineering to ever growing IoT systems and challenges they provide.(L2)

Unit III

IoT and M2M : M2M, Difference between IOT andM2M, SDN and NFV for IOT, Software defined Networking, Network FunctionVirtualization, Need for IOT Systems Management, Simple Network Management Protocol,Limitations of SNMP, Network Operator Requirements, NETCONF, YANG, IOT Systemsmanagement with NETCONF-YANG.

Learning Outcomes:

At the end of the unit, the student will be able to

- To summarize the machine to machine communication in a network under IoT design.(L2)
- To simulate the network of things with various IoT related systems.(L2)
- To extend the requirements of a system under IoT for different specialized operations management.(L2)

Unit IV

Internet of Things Systems - Logical Design using Python: Introduction, Motivation for using Python, Installing Python, Python Data Types & Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date/ Time Operations, Classes, Python Packages of Interest for IoT.

Learning Outcomes:

At the end of the unit, the student will be able to

- To apply the knowledge of Python programming to IoT system design.(L3)
- To Outline different packages useful for IoT application development.(L2)

Unit V

IOT Physical Devices & Endpoints: What is an IOT Device, Exemplary Device, Board, Linux on Raspberry Pi, Interfaces, and Programming with Python, other IoT devices.

IoT Physical servers & Cloud Offerings:

Introduction to cloud storage models & communication APIs, python web application framework-Django, Designing a REST ful web API, Amazon web services for IoT.

Learning Outcomes:

At the end of the unit, the student will be able to

- To outline the cloud storage and server options with various Communication APIs.(L2)
- To relate Amazon Web services for IoT system development.(L2)
- To explain the Django framework for python based web application development.(L2)

Text Books

1. Vijay Madisetti, Arshdeep Bahga, Internet of Things A Hands-On- Approach,2014.

References

1. Matt Richardson & Shane Wallace, Getting Started with Rasperry Pi, O'Reilly (SPD), 2014.
2. Adrian McEwen, Designing the Internet of Things, Wiley Publishers, 2013
3. Daniel Kellmereit, The Silent Intelligence: The Internet of Things, 2013

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1205.1	Communication Network Processors	3	0	3

Course Objective:

- Learn how computer network hardware networking
- Apply their foundations in software engineering to adapt to readily changing environments using the appropriate theory, principles and processes
- Introduce the student to advanced networking concepts, preparing the student for entry Advanced courses in communication networking.
- Describe features, benefits, and functions of Cisco ASR 1000 Series routers

Course Outcomes:

At the end of the course, the student will be able to

1. understanding of the basic concepts of data communications including the key aspects of networking and their interrelationship, packet switching, circuit switching and cell switching as internal and external operations, physical structures, types, models, and internetworking(L2)
2. apply the software engineering lifecycle by demonstrating competence in communication, planning, analysis, design, construction, and deployment(L3)
3. Demonstrate the ability to unambiguously explain networking as it relates to the connection of computers, media, and devices (routing).(L2)
4. evaluate the performance of a single link, logical process-to-process (end-to-end) channel, and a network as a whole (latency, bandwidth, throughput).(L5)
5. Discuss the architecture, features, and functions of the hardware elements of the Cisco ASR 1000 Series chassis, route processor, embedded services processor (ESP), QFP Buffer.(L6)

Unit I

Overview of Data Networks: End point: Data Modems, Serial interfaces, ISDN interface – Communication: Types of switching, Types of error: single and burst error, Error detection, redundancy check: Longitudinal, vertical, and cyclic error correction, architecture of computer network - Overview of OSI reference model – Network components: Routers, Bridges and Gateways.

Learning Outcomes:

At the end of the unit, the student will be able to

- outline the overview of data networks (L2)
- explain the how the process of error detection and correction in data networks.(L2)

Unit II

Communication Software Design: Ecosystem - embedded communications software - software partitioning - module and task decomposition - Partitioning case study - Protocol software - debugging protocols - tables and other data structures - table access routines - Buffer and timer management

Learning Outcomes:

At the end of the unit, the student will be able to

- Explain about the embedded communications software(L2)
- Understand the debugging software protocols.(L2)

Unit III

Management software – device & router management – CLI based management & HTTP based management - Agent to protocol interface – device to manager communication – system setup, boot & post-boot configuration – saving and restoring the configuration.

Learning Outcomes:

At the end of the unit, the student will be able to

- Compare CLI based management & HTTP based management.(L2)
- Discuss the process of device to communication manager.(L2)

Unit IV

Multi-Board Design: Multiboard common architectures for communication equipment – Single board, chassis and rack-based designs - Components of a multi board designs – RTOS support for distribution – data structure and state machine changes for distribution – failures and fault tolerance in multi board systems.

Learning Outcomes:

At the end of the unit, the student will be able to

- outline the Multiboard common architectures for communication equipment.(L2)
- explain the RTOS support for distribution.(L2)

Unit V

Design Principles Of Scheduling: Processor scheduling – Multiprocessor scheduling – Limited packet processing capacity in routers – real time scheduling on multiprocessors – Multithreaded Packet processors – random external memory accesses.

Communication Processor Architectures: The TRIBE Architecture – Tribe pipeline – Quantum Flow Processor - Introduction – Architecture of quantum flow processor – ASR 1000 series router – QFP residing on distributed line cards – High level packet flow – Packet Processors Engines – Packet Processor Engine resources - QFP Buffer, Queue and scheduling.

Learning Outcomes:

At the end of the unit, the student will be able to

- Discuss the various types of communication processor architectures (L2)
- Explain the function of Quantum Flow Processor..(L2)
- Outline the concepts of Buffer, Queue and scheduling.(L2)

Text books

1. Behrouz A. Forouzan, “Data Communications and Networking”, 4th Edition, Mc-Graw Hill.
2. T. Sridhar , “Designing Embedded Communications Software”, CMP books, 2003.
3. Mark A. Franklin, Patrick Crowley, HaldunHadimioglu and Peter Z. Onufryk., “Network Processor Design – Issues and Practices”, Elsevier, 2005.
4. “The CISCO Quantum Flow Processor”, CISCO’s Next Generation Network Processor Manual.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1205.2	Embedded Wireless Sensor Networks	3	0	3

Course Objectives:

- Emphasize the basic WSN technology and sensor node architecture with unique constraints and challenges in design of WSN for different Applications.
- Summarize the network architecture and the network principles towards sensor networks.
- Provide the sensor network implementation using the prominent tools and operating system.
- Explain the programming concepts for cooperating nodes and networks.
- Show the applications of sensor network and development in society.

Course outcomes:

At the end of the course, the student will be able to

1. Illustrate the wireless sensor and network definitions, advantages, constraints, challenges and sensor node architecture with applications.(L2)
2. Explain the network architecture and its requirements needed for embedded wireless sensor networks.(L2)
3. Demonstrate the embedded wireless sensor network programming and operating system capabilities using tiny OS.(L2)
4. Interpret the programming models and network architecture structure programming for embedded wireless sensor network.(L2)
5. Illustrate the tools to implement the programming and networking on a wireless sensor network.(L2)

Unit I

Introduction to WSN: Introduction to WSN-Challenges for WSNs - Characteristic requirements - Required mechanisms - Single-node architecture -Hardware components Energy consumption of sensor nodes-Operating systems and execution environments-Some examples of sensor nodes.

Learning Outcomes:

At the end of the unit, the student will be able to

- Illustrate the challenges and characteristics for WSN (L2).
- Identify the Hardware components Energy consumption of sensor nodes-Operating systems and execution environments.(L3)

Unit II

Network Architecture: Sensor network scenarios- Optimization goals and figures of merit- Design principles for WSNs, Service interfaces of WSNs- Gateway concepts.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the design principles of Network architecture (L2).
- Explain the service interface and gateway concepts.(L2)

Unit III

Sensor Network Implementation: Sensor Programming- Introduction to TinyOS Programming and fundamentals of Programming sensors using nesC- Algorithms for WSN – Techniques for Protocol Programming.

Learning Outcomes:

At the end of the unit, the student will be able to

- Design a sensor programming on tiny OS (L6).
- Explain theprotocol programming techniques.(L2)

Unit IV

Programming Models: An Introduction to the Concept of Cooperating Objects and Sensor Networks-System Architectures and Programming Models.

Learning Outcomes:

At the end of the unit, the student will be able to

- Interpret the Concept of Cooperating Objects and Sensor Networks (L2).
- Explain the System Architectures and Programming Models.(L2)

Unit V

Case Studies: Wireless sensor networks for environmental monitoring, Wireless sensor networks with mobile nodes, and Autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.

Learning Outcomes:

At the end of the unit, the student will be able to

- Apply Wireless sensor networks for environmental monitoring(L3).
- Analyse the Wireless sensor networks with mobile nodes, and Autonomous robotic teams for surveillance and monitoring.(L2)

References

1. Holger karl, Andreas Willig, “Protocols and architectures for wireless sensor networks”, John Wiley,2005.
2. 2.LiljanaGavrilovska, SrdjanKrco, Veljko Milutinovic , Ivan Stojmenovic,RomanTrobec, “Application and Multidisciplinary Aspects of Wireless Sensor Networks”, Springer-Verlag, London Limited 2011.
3. Michel Banâtre, Pedro José Marrón, Anibal Ollero, Adam Wolisz, ”Cooperating Embedded Systems and Wireless Sensor Networks “, John Wiley & Sons, Inc .2008.
4. Seetharaman Iyengar, Nandhan, “Fundamentals of Sensor Network Programming Applications and Technology” , John Wiley & Sons, Inc.2008.

I Year –II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1205.3	Principles of Distributed Embedded Systems	3	0	3

Course Objectives:

- To make the student gain proficiency in designing distributed embedded systems.
- To understand the real time problems on devices
- To understand the scheduling and designing of static and dynamic systems
- To make the working of controlled area network
- To understand the CAN configuration files.

Course Outcomes:

At the end of the course, the student will be able to

1. Conceptualize system from given requirements.(L2)
2. Design real time models. (L6)
3. Apply real time components like real time networking, real time OS, in the design of embedded systems.(L3)
4. Understand CAN protocol system and standard quality.(L2)
5. discuss the CAN standards for network management.(L6)

Unit I

Real-Time Environment: Real-time computer system requirements – classification of real time systems – simplicity – global time – internal and external clock synchronization – real time model. Real – time communication – temporal relations – dependability – power and energy awareness – real –time communication – event triggered – rate constrained – time triggered.

Learning Outcomes:

At the end of the unit, the student will be able to

- classify of real time systems (L3).
- Understand the power and energy awareness in a real time enviroment .(L2)

Unit II

Real-Time Operating Systems: Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand Inter component communication process (L2).
- Explain the task management.(L2)

Unit III

System Design: Scheduling problem - static & dynamic scheduling – system design – validation – time–triggered architecture.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the importance of scheduling problem in system design (L2).
- Explain the time triggered architecture.(L2)

Unit IV

Introduction To Can: Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the CAN protocol opeatations (L2).
- Compare CAN protocol to other serial communication protocols.(L3)

Unit V

CAN Standards: Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder.

Learning Outcomes:

At the end of the unit, the student will be able to

- Understand the CAN standards(L2).
- Explain theDevice Profile Encoder.(L2)

References

1. Hermann Kopetz, “Real–Time systems – Design Principles for distributed Embedded Applications”, 2nd Edition, Springer 2011.
2. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Copperhill Media Corporation, 2008.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1206.1	Memory Technologies	3	0	3

Course Objectives:

- To introduce about various type of memory Architectures.
- To introduce about various performance parameter of memory Architectures.
- To introduce about various memory packing technologies.
- To introduce about various 2D & 3D memory Architectures

Course Outcomes:

At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know how of the state-of-the-art memory chip design
4. Understand about various memory packing technologies.
5. Understand about various 2D & 3D memory Architectures

Unit I

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific, SRAMs.

Unit II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced, DRAM Design and, Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

Unit III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs Floating Gate, EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit IV

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit V

Advanced Memory Technologies and High-density Memory Packing Technologies:, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog, Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory, Devices.

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards,High Density Memory Packaging

Text Books

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1206.2	Low Power VLSI Design	3	0	3

Course Objectives:

- Study the MOS transistor modelling is emphasized for low power applications
- Study the modelling of various MOS parameters and SPICE simulation for low power applications,
- Discuss the Relationship of probability while calculating power dissipation of circuits
- Outline Power reduction techniques possible at circuit ,logic level
- Examine Clock as a major source of power dissipation and distinguish various methods to reduce it

Course Outcomes:

At the end of the course, the student will be able to

1. Analyse the need for low power VLSI circuits(L4)
2. Understand dynamic and static power dissipation and factors affecting them(L2)
3. Identify the Role of simulation possible at various levels of design(L3)
4. Apply Power reduction techniques possible at circuit ,logic level(L3)
5. Analyse Clock as a major source of power dissipation and distinguish various methods to reduce it(L4)

Unit I

Fundamentals of Low Power VLSI Design: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

Learning outcomes:

At the end of the unit, the student will be able to

- Understand the concept of Low power circuit design (L2)
- Discuss various ways power dissipating in the.(L4)

Unit II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

Learning outcomes:

At the end of the unit, the student will be able to

- Understand switched capacitor minimization Approaches.(L2)
- Compare different Circuit Level Measures, Mask level Measures. .(L4)

Unit III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

Learning outcomes:

At the end of the unit, the student will be able to

- Illustrate the concepts of CMOS Adder's Architectures.(L2)
- Apply theLow-Voltage and Low-Power Logic Styles. (L4)

Unit IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Learning outcomes:

At the end of the unit, the student will be able to

- Understand the need of low power in multiplication techniques.(L2)
- Introduce the different types of multipliers

Unit V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Learning outcomes:

At the end of the unit, the student will be able to

- Illustrate the concepts of ROM.(L2)
- compare different Low-Power SRAM Technologies.(L4)

Text Books

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1206.3	CAD of Digital Systems	3	0	3

Course Objectives:

- To introduce different VLSI design methodologies.
- To introduce VLSI automation tools.
- To learn the basics of general purpose methods for optimization.
- To learn the concept of simulation & synthesis and implementation of simple circuits using RTL.

Course Outcomes:

At the end of this course, students will be able to

1. Understand the Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
2. Compare various phases of CAD, including simulation, physical design, test and verification.
3. Demonstrate knowledge of computational algorithms and tools for CAD
4. Apply simulation and synthesis process on various digital systems
5. Implement a simple digital circuits using VHDL/Verilog

Unit I

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices,
Fabrication, Process and its impact on Design.

Unit II

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Unit III

General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement , routing.

Unit IV

Simulation – logic synthesis, verification, high level Synthesis.

Unit V

MCMS-VHDL-Verilog implementation of simple circuits using VHDL

Text books

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.
2. S.H. Gerez, “Algorithms for VLSI Design Automation.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
EC- ESVD1207	Embedded Systems Lab	3	0	3

Course Objectives:

- To impart the basic instructions of ARM-926 for implementation of arithmetic, logical, BCD and ASCII operations.
- To Demonstrate various string, branching and process control instructions for implementation of ARM cortex.
- To Explain the mechanism of RTOS based interrupt handling services with demonstrated examples.
- To Explain the process of interfacing AMR CORTEX microprocessor with peripheral control ICs .
- To Explain the procedure of interfacing AMR CORTEX microcontroller with timers, parallel and serial communication ports.
- To Demonstrate the usage of AMR CORTEX as embedded controller with real world applications like calculator, LCD and hex keypad etc.

Course Outcomes:

At the end of the course, the student will be able to

1. Develop programming skills for data operations and different interfacing circuits of ARM-926.(L6)
2. Develop ARM-926 to demonstrate the arithmetic operations of . Interrupt handling. Allocate resource using semaphores.. Share resource using MUTEX(L6)
3. Examine different string, branch and process control based operations in assembly language such as moving string, finding length of string, reverse of string, insertion, deletion, sorting.(L3)
4. Explain the process of interfacing **ARM-CORTEX** with peripheral control ICs (L2)
5. Develop RTOS programs to make use of parallel ports, timers and serial port of embedded sytem(L6)

Note:

- The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926developer kits and ARM-Cortex.
- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification.
- The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments

Part-I: Experiments using ARM-926 with PERFECT RTOS:

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II Experiments on ARM-CORTEX processor using any open source RTOS.

(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

1. Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library,
2. COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
3. LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

1. The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
2. Serial Cables, Network Cables and recommended power supply for the board.

I Year -II Semester

Subject Code	Subject Name	L	P	Credits
AC- RMIP1201	Research Methodology and IPR	2	0	0

Course Objectives:

At the end of this course, students will be able to

- Introduce the research problem formulation.
- Learn research related information Follow research ethics
- Introduce the when IPR would take such important place in growth of individuals & nation, it is needless to emphasise the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Introduce the IPR protection provides an incentive to inventors for further research work and investment in R & D.

Course Outcomes:

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information and Follow research ethics
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasise the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits

Unit I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit II

Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit III

Effective technical writing, how to write report, Paper, Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall , "Industrial Design", McGraw Hill, 1992.
6. Niebel , "Product Design", McGraw Hill, 1974.
7. Asimov , "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.

9. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

Main Project-I,II

Course Outcome:

After successful completion of the course, student will be able to

- Apply various tools and techniques to study existing systems.
- analyse existing systems, thereby select and justify parameters to be improved
- Design proposed engineering solution as per industry / research / societal need
- Obtain precision in uses of the tools related to their experiments/fabrication
- Compare various components of technology to optimize the resources at large
- Appraise the potential of technology for scalability and wide spectrum of applications
- Report project related activities effectively to peers, mentors and society

Syllabus: The major project shall be based on the recent trends in technology, system/process analysis, construction/fabrication/production techniques, design methodologies etc. The student(s) shall carry out a comprehensive project at relevant Academic/R&D/Industrial organisation based on one or more of the following aspects: prototype design, product preparations, working models, fabrication of set-ups, laboratory experiments, process modification/development, simulation, software development, integration of software and hardware, data analysis, survey etc. The student is required to submit comprehensive project report based on the work and publish their work in national/ international conferences or journals.